A 58dB SNR 6th Order Broadband 10.7 MHz SC Ladder Filter

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Abstract
A 6th order 10.7 MHz bandpass switched-capacitor ladder filter achieving 58 dB signal to noise ratio is presented. Filter is based on an Operational Transconductance Amplifier (OTA) that presents both good accuracy and high slew-rate. The use of several techniques minimizes the capacitance spread. The passband ripple is less than 1 dB. The IM3 is –40 dB for a two tone input signal with a power of +3 dBm power level each. The chip was fabricated in a 0.35 μm CMOS process.

Introduction
Most of the high performance filters in the audio and video systems are based on switched-capacitor techniques (1)-(4), as well as sigma-delta modulators and data converters. For high-speed applications, the switch delay has to be minimized, and the operational amplifier must be able to settle to the final value within few nanoseconds. For high-Q filters, the scenario is more complex because the large capacitive spread (proportional to Q) required.

Recently, several design techniques for SC filters in the range of 10 MHz have been reported (1)-(3). Efficient narrow-band filters based on N-path technique have been reported, but to use those techniques for broadband, small passband ripple and ladder filters is more complicated. N-path filters suffer from spurs images due to mismatches in the different filter trajectories; this issue might be overcome using randomization techniques (3). Since many building blocks use slower clocks, the effective sampling rate reduces according to the number of path trajectories; hence the antialias filter is more complex. Techniques based on the cascade of biquadratic sections usually results in a filter realization with lower capacitance spread, but its sensitivity to component tolerances in comparison to ladder filters is higher. In this work, a double terminated ladder filter is designed; the main specs are: f_0=10.7 MHz, BW=400 kHz, passband ripple of 1 dB, and clock frequency of 62.5 MHz.

Design Considerations for the OTA
In SC circuits we have to consider two switches, hence the time constant is $2R_sC$. This effect however, is partially absorbed by the limited speed of the OTA; the effective delay introduced by the switch resistance is around 1.5-3 times R_sC.

The settling time of an OTA-C circuit has three different regions of operation. If the voltage across the input differential pair is greater than the overdrive voltage, the amplifier slews. The slewing time is determined by the amount of current the amplifier delivers to the load capacitor. As the voltage across the differential pair drops, the amplifier enters into its linear settling regime. The time-constant of the amplifier in this regime depends on Gain-Band-Width product (GBW) and Phase Margin (PM); it is also determined by the closed loop arrangement of capacitors. Fig. 1a shows various capacitors connected to the OTA at a given clock phase. C_F, C_I, and C_L denote the feedback, input and load capacitors, respectively. C_P accounts for the parasitic capacitors lumped to the OTA inverting input.

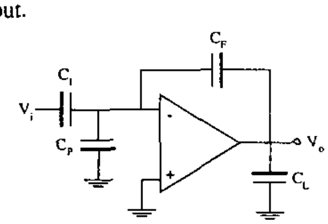

Fig. 1. Typical configuration present in a SC filter.

The slew-rate of the integrator is determined according to:

$$SR = \frac{I_{OMAX}}{C_{L\_eff}} \tag{1}$$

where I_{OMAX} stands for the maximum OTA output current and C_{L_eff} is the effective load capacitance, given by

$$C_{L\_eff} = C_L + \frac{1}{\frac{1}{C_F} + \frac{1}{C_I + C_P}} \tag{2}$$

Hence it is desirable to reduce C_{L_eff}. The capacitors set the feedback factor β, and the closed-loop pole becomes

$$\omega_{eff} = \frac{\beta g_m}{C_{L\_eff}} = \left(\frac{C_F}{C_F + C_I + C_P}\right)\frac{g_m}{C_{L\_eff}} \tag{3}$$

where g_m is the OTA transconductance. We have little choice in selecting the capacitor values C_I, C_F, and C_L since they are set by the minimum capacitance and filter specifications. The only option is arranging the switching phases of each amplifier such that the effective load capacitance is reduced. Sampling the OTA output during the integrator's hold phase increases both ω_{eff} and SR. It is also important to minimize the C_P, especially if it is comparable to C_I and C_F.

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OTAs for SC Filters

The folded-cascode OTA is commonly used in SC applications. It achieves a dc gain of the order of $(g_m r_o)^2$, which is inversely proportional to the bias currents. For high-speed designs requiring large bias currents the dc gain is limited to 40~50 dB. Its single non-dominant pole is at the source of the cascode transistors. A major drawback of this topology is its relatively non-efficient slew-rate, since the maximum current delivered to the load capacitor is around 50% of the whole OTA dc current.

In the complementary folded-cascode, two differential pairs are used to exploit both cascode transistors (4)-(5). The low-frequency transconductance is composed by the concourse of the two differential pairs. The two feed-forward signal paths create a zero, which partially compensates the phase degradation due to the two non-dominant poles. A greater fraction of the total bias current is steered to the load; for same power consumption and same transconductance, this OTA achieves around 33 % higher SR and a bit smaller phase margin as compared with the folded-cascode structure (5).

The advantages of using OTAs with several paths have being pointed out in (4). Shown in Fig. 2 is a three-path OTA. A folded-cascode OTA is implemented due to the action of M1, M2 and M3, and a current-mirror cascode OTA is composed by transistors M1, M2, M3 and M6. Also, a current-mirror folded-cascode OTA is embedded due to M1, M4, M6 and M7. M6 is the basic transistor of the current mirror: one of its copies, M2, folds to the output stage with a gain of N; the other copy, M7, provides a current gain of M. The non-dominant poles are lumped to the cascode transistors M3 and M4, and to the gate of M6. The small-signal transconductance is given by:

$$G_m = \frac{g_{m1}}{1+\frac{s}{\omega_{N1}}} + \frac{Ng_{m1}}{\left(1+\frac{s}{\omega_{N1}}\right)\left(1+\frac{s}{\omega_{N2}}\right)} + \frac{Mg_{m1}}{\left(1+\frac{s}{\omega_{N2}}\right)\left(1+\frac{s}{\omega_{P1}}\right)} \quad (4)$$

with

$$\omega_{N1} \cong \frac{g_{m3}}{C_{GS3}+C_{SB3}}; \quad \omega_{N2} \cong \frac{g_{m6}}{C_{GS6}(1+M+N)}; \quad \omega_{P1} \cong \frac{g_{m4}}{C_{GS4}+C_{SB4}} \quad (5)$$

The pole at ω_{N2} is the most important one. The topology tolerates to locate the closed-loop unity gain frequency close to ω_{N2} because the feed-forward paths generate 2 zeros. The OTA output current is a greater fraction of the total current, as all transistors except M5 adjust dynamically their currents during slewing. This OTA presents larger DC gain and enhanced SR, but its phase margin is not as good as that of the folded-cascode OTA. This OTA has smaller input transistor sizes, with reduced input capacitances; as a result, its closed-loop response is faster provided that the phase margin is good enough. This topology is noisier because of the lower transconductance of the input stage; this is not critical for SC circuits wherein the most important noise contributions are due to the switch resistance and filter's Q.

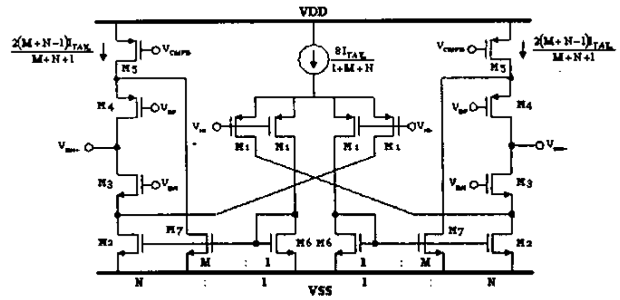

Fig. 2. Three-Path OTA.

The OTAs are compared for same transconductance, same power consumption and same output swing with 2 pF capacitors. The results are grouped in table I; the three-path OTA was designed with current-mirror gains of N=4 and M=1. The complementary differential pair and the three-path OTA achieve the highest DC gain because of the reduced bias current in their cascode transistors and extra signal paths. During slewing the three-path OTA outperforms the other topologies. Table I also shows that the three-path OTA achieves the lowest settling error (0.28 %).

Table I. OTAs comparison. Gm=4.2 mS for all structures.

Parameter	Folded-cascode	Complementary pairs	3-path OTA
DC gain [dB]	55.9	60.6	60.4
SR [V/μs]	125.	194.4	219.
Ts[1%] [ns]	5.22	3.30	3.60
Ts[0.1%] [ns]	7.46	5.03	5.49
Settling error [%]	1.04	0.40	0.28
noise [nV/Hz$^{1/2}$]	1.67	1.73	2.43

Filter Design

The passive elements of the filter prototype can be obtained from tables or available software packages. The 6[th] order filter consists of three coupled (through QC) resonators terminated with switched capacitors γC as shown in Fig. 3. The frequency of the resonators is determined by the capacitors θC ($\theta \cong 2\pi f_0/f_s$); Q filter terminations are computed as:

$$Q = \frac{BW}{\omega_0}\frac{1}{\sqrt{L_2 C_1}} \; ; \; \gamma = \left(\frac{BW}{\omega_0}\frac{1}{C_1}\right)\theta \quad (6)$$

BW is a unitless parameter equal to the filter bandwidth and ω_0 is the center frequency in rad/sec. C_1 and L_2 are the elements of the passive LP-filter prototype. Usually L_2C_1 is greater than unity hence the capacitor spread is large, roughly 32 for this design. The capacitors needed for this filter are shown in table II.

Table II. Capacitor values for the 6th order ladder filter.

	Typical design	Secondary clock (N=4)
$\alpha = Q$	1/32	1/8, 1.25/8 *
γ	1/32	1/8
θ	1	1
Total capacitance	782 C_u	219 C_u

*These capacitors are implemented as shown in Fig. 4a.

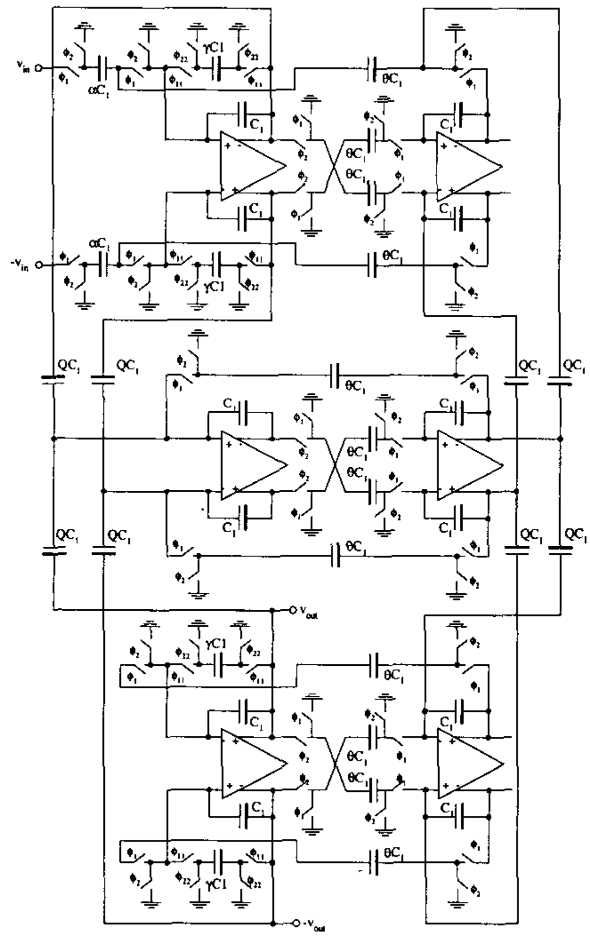

Fig 3. Schematic of the 6th order bandpass filter.

Several techniques are used to reduce the capacitance spread. By using two capacitors of $1.25\delta C$ and δC, as shown in Fig. 4a, the charge of the capacitors is partially cancelled, leading to an effective capacitor of $\delta C/4$. This technique is also used for the realization of capacitors αC_1 and QC_1. If the input signal of a SC integrator is sampled once every N-periods, the amount of charge driven is N-times lower, and the equivalent resistance increases by factor N (6). The basic concept is shown in Fig. 4b for N=4. This results in lower capacitance spread without sacrificing sensitivity to component variations. Table II shows the capacitance values for the design using these techniques.

For fast response, it is required that the input to each integrator is as close as possible to a step function and to minimize the load capacitor during the integration phase. This can be best done by using forward integrators and by crossing the outputs, as shown in Fig. 3.

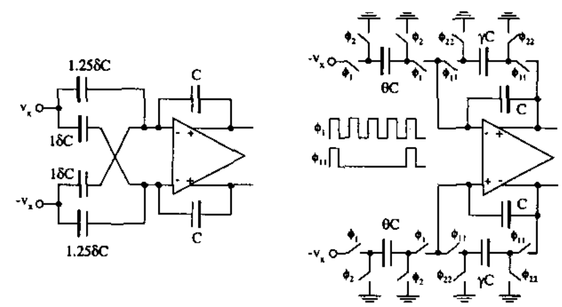

Fig. 4. Reduction of the capacitor spread: a) charge cancellation b) slower clock; ϕ_{11} and ϕ_{22} operate at $f_s/4$.

Experimental Results

The OTA and a 6th-order bandpass filter has been fabricated in the TSMC 0.35 μm technology through the MOSIS educational service. The chip microphotograph is shown in Fig. 5; active area is 0.84 mm^2. An open drain differential pair is used to drive 50Ω power combiners at the output; its attenuation was measured to be around –30 dB. Fig. 6 shows the magnitude and phase response of the filter. The low-frequency response is limited by the balun. The filter's passband gain is around –3.8 dB while the passband ripple is less than 1 dB. The center frequency shows a 0.5 % shift from the ideal frequency, which is in agreement with the expected results. The third intermodulation distortion is around –46 dB for a two tone input signal of 0 dBm each; the results are shown in Fig. 7. Measured IM3 for the standalone buffer is around –55 dB for same input tones. The filter's noise density is –139 dBm/Hz$^{1/2}$, as shown in Fig. 8. Measured SNR is 52 dB for IM3=–46 dB, and 58 dB for IM3=-40 dB. Table III lists the experimental results together with previously published filters.

Conclusions

A 10.7 MHz 6th-order SC ladder filter was reported. The filter employs a multi-path OTA with enhanced SR and small input capacitance properties. The capacitor spread was reduced by more than 70 % by using charge cancellation techniques and slower clocks. Although the frequency of the slower clocks used is only 15 Mhz the image signals are attenuated by more than 45 dB. The filter dynamic range is around 58 dB and the passband ripple is less than 1 dB for the whole 400 kHz bandwidth. IM3 is below –40 dB for a two tone input signal of +0 dBm power level each.

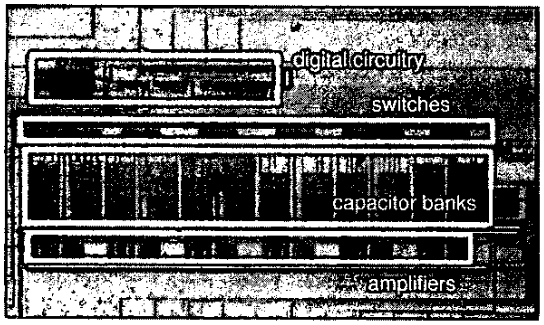

Fig. 5. Chip microphotograph of the SC-filter and OTA.

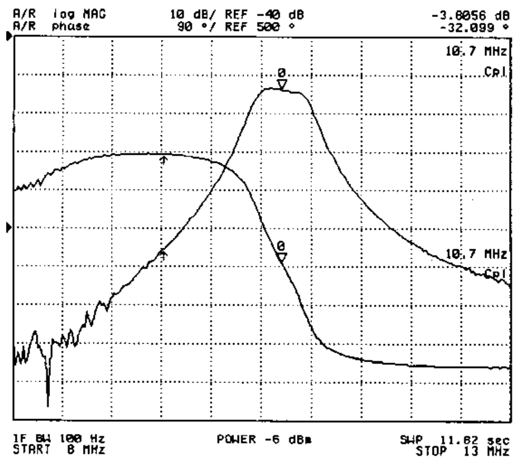

Fig. 6. Magnitude and phase response for the filter.

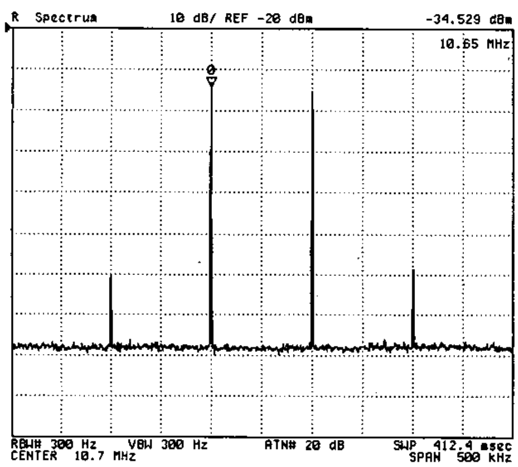

Fig. 7. Third intermodulation filter results.

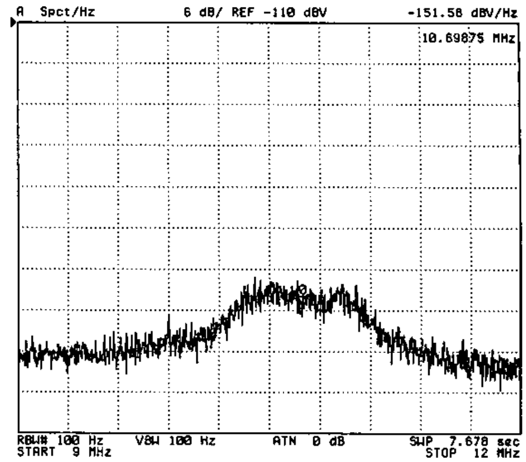

Fig. 8. Measured output referred noise level.

Table II. Comparison of filter performances.

	[1]	[3]	This work
Technology	1.2μm BiCMOS	0.6μm CMOS	0.35μm CMOS
Filter type	Biquad	Multipath	Ladder
Filter order	2	6	6
f_0 [MHz]	10.7	10.7	10.7
BW [kHz]	369	195	464
Ripple [dB]	3	3	1
Output noise [V_{rms}]	707	226	295
DR (IM3=-40 dB) [dB]	58	61	58
Supply voltage [V]	3.0	3.3	3.0
Power-per-pole [W]	11.5 m	2 m	9 m

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