FULLY-INTEGRATED LC VCOS AT RF ON SILICON

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ABSTRACT

Fully integrated negative conductance Voltage Controlled Oscillator (VCO) design examples at GHz frequencies in Si BiCMOS and CMOS technologies are provided. The advantages and shortcomings of the structures are briefly presented together with the associated design trade-offs. Phase noise of a CMOS VCO is calculated based on the Linear Time-Variant Impulse Sensitivity Function (ISF) theory and compared to the simulations. Experimental results of two fully integrated CMOS VCOS designed with 0.5μm and 0.35μm CMOS technologies at 2.2GHz are given.

I. INTRODUCTION

VCOs are among the key building blocks of wireless communication systems. The quality of the VCO is vital in setting the performance of the PLL-based frequency synthesizers used in generating the Local Oscillator (LO) signals that convert the transmitted and received information signals in frequency. The trend toward low cost and large scale integration in wireless communications systems design steadily increases the demand for fully integrated VCOs at RF in CMOS and BiCMOS technologies. Negative conductance based differential VCO structures using integrated spiral inductors and varactors as resonators show promising results as more and more efforts are put on improving the quality of the integrated resonator passive elements by the designers and process developers, [1]-[6]. After briefly emphasizing the impact of the VCO quality on the performance metrics of PLL-based frequency synthesizers in Section II, this paper focuses on design examples of negative conductance LC VCOS in Si BiCMOS and CMOS technologies in Section III, where the advantages and shortcomings of the structures are presented together with the associated design trade-offs. In Section IV, experimental results of two CMOS VCOS are given. Finally, some conclusions are drawn in the last section.

II. VCO IN A PLL

PLL is a widely used building block in modern communication systems, mostly in synthesizing well-defined, stable local oscillator signals for up and down-converting the transmitted and received signals, respectively, [7]. It is well accepted that the most challenging parts of especially high-frequency PLLs used in wireless communication systems are the VCOs due to the very stringent low noise specifications with low power consumption at GHz frequencies. The increasing demand for complete integration in relatively low cost IC technologies, i.e. CMOS, BiCMOS, without any performance compromise, as the frequency of operation increases steadily complicates the design even further.

![Phase-Locked Loop Diagram](image)

Figure 1: Phase-Locked Loop: (a) Basic block diagram, (b) Phase noise of a first-order loop with a low noise input

Block diagram of a first-order PLL is shown in Fig.1(a). A reference signal usually from a low noise crystal oscillator is compared with the divided VCO signal by the Phase Detector (PD) and the resulting signal after low-pass filtered is connected to the VCO as the control voltage, closing the loop. When
the loop is in locked condition, the output frequency of the PLL, i.e. the output frequency of the VCO, becomes equal to the reference frequency multiplied with the divider ratio, that is $\omega_o = N \cdot \omega_{ref}$. The demanding phase noise specifications of wireless communication standards sets the major design challenge as achieving low noise at the PLL output. The phase noise of a first-order PLL with a low noise input is depicted in Fig.1(b) for the sake of illustrating the effect of the VCO phase noise on the output noise of the overall PLL system, [4]. Note that, even though the VCO phase noise at offset frequencies lower than the loop bandwidth is suppressed by the loop, the phase noise of the PLL is determined by that of the VCO at offset frequencies larger than the loop bandwidth, denoted as $\omega_{loop}$. On the other hand, the need for synthesizing frequencies with small steps limits the loop bandwidth to small values, [7], thus the VCO phase noise remains unsuppressed at the output of the PLL for some large offset frequencies where the specifications of wireless standards are demanding. This clearly shows the importance of low noise VCO design for a high-performance frequency synthesizer complying with the standards.

III. NEGATIVE CONDUCTANCE VOLTAGE-CONTROLLED OSCILLATORS

Negative conductance voltage-controlled oscillators are by far the most widely used VCO structures in GHz range designs. The simplicity of the structure that allows the generation of a differential negative conductance with only two transistors in the signal path makes the circuit very attractive for applications where low noise with low power consumption at GHz range are key performance metrics.

The basic negative conductance VCO is depicted conceptually in Fig.2(a). The inductor and the variable capacitor form the resonator tank, and the conductance $G_{loss}$ represents the loss due to the finite quality factor of the resonator. The negative conductance is denoted as $-G$ in the illustration. A sample circuit implementation in CMOS is shown in Fig.2(b), where the differential oscillator is built with symmetry around the resonator tank. The negative conductance $-G$ generated by the cross coupled NMOS transistors $M_1$ and $M_2$ is designed to compensate for the loss associated with the LC tank. It can be shown that the negative-conductance seen differentially at the drain of the NMOS transistor is $-G \approx -g_m/2$, where $g_m$ denotes the transconductance of each transistor. In order for the oscillations to be sustained in the circuit, the tail current of the cross coupled transistor pair should be increased to a level high enough for the negative conductance to be larger in absolute value than the equivalent loss of the tank.

A. Bipolar VCO Design

In this section, some design trade-offs involved in the design of Bipolar negative conductance VCOs are briefly provided. The schematic of a Bipolar VCO is shown in Fig.3. The cross coupled transistors $Q_1$ and $Q_2$ generate the negative conductance required to compensate for the loss associated with the finite quality factor of the LC tank which sets the frequency of oscillation.

![Figure 3: Bipolar Voltage-Controlled Oscillator](image)

The tank varactor is a reverse-biased PN junction available in the 0.6 $\mu$m BiCMOS technology used in the design. It can also be the base-emitter or base-collector junctions of a bipolar transistor used...
in reverse-bias, [5]. The emitter-degeneration resistors $R_{E1}$ and $R_{E2}$ are used to reduce the upconversion of noise around the carrier at low offsets by linearizing the negative conductance generator, [2]. Care should be taken in optimizing the value of the resistors through phase noise simulations as their thermal noise contribution at large offsets may degrade the phase noise. Another important concern is that the addition of the degeneration resistors reduces the loop gain. Thus the start-up of the oscillations should be guaranteed over the process variations. The capacitive coupling through $C_{c1}$ and $C_{c2}$ in the feedback of the cross coupled transistors $Q_1$ and $Q_2$ is used to avoid the clipping at the output swing due to the saturation of the transistors. The simulations show that the voltage swing at the output of the VCO is almost doubled with capacitive coupling as compared to direct coupling. As a consequence, the phase noise is improved considerably since it is inversely proportional to the voltage swing,[4]; more than 8 dB improvement at 600kHz offset is observed in the SpectreRF simulations of the VCO designed to operate at around 2.5 GHz. Note that, capacitive coupling also reduces the loop gain through capacitive division. Careful design of the capacitive coupling is therefore vital to ensure the oscillations. It is also important to minimize the phase noise contribution from the bias resistors $R_{B1}$ and $R_{B2}$, [5]. The cross coupling in the negative conductance generating transistors can also be done through emitter followers in lieu of the capacitors, [2]. Although the resulting structure also proves useful in preventing the amplitude clipping that occurs due to the forward biased base-collector junction, the additional power consumed by the emitter followers and their phase noise contribution may be a concern. The biasing of the VCO core shown in Fig.3 is supplied by a bandgap bias generator that feeds the tail current mirror. The phase noise contribution of the bias generator through upconversion of low frequency noise around the carrier can be significant, requiring proper measures to be taken to design the bias circuit for low noise.

B. CMOS VCO Design

The emphasis in this section is put on analytically calculating the phase noise of a CMOS VCO designed with HP 0.5μm CMOS Technology, based on a time-variant phase noise theory, [8]. The theory proves useful to calculate the contributions of each component in a VCO to the phase noise, [3], thus allowing for optimization in the design process. Schematic of the CMOS VCO with complementary cross coupled transistors around an LC tank is shown in Fig.4.

![Figure 4: CMOS Voltage-Controlled Oscillator](image)

The negative conductance generating cross coupled NMOS and PMOS transistors, $M_1$-$M_4$ are designed to compensate for the loss associated with the LC tank. The advantage of using both PMOS and NMOS cross coupled transistors is mainly two-fold: first, with the addition of the PMOS cross coupled pair, it is possible to compensate for the loss of the tank with less current consumption saving some power, [1], and second by observing the symmetry properties of the oscillating waveform sizing the PMOS and NMOS transistors ($g_{mp} = g_{mn}$), it is possible to reduce the upconversion of $1/f$ noise of the transistors around the carrier, thus lowering the phase noise, [4]. On the other hand, it is obvious that the additional headroom required for the biasing of the PMOS transistors as compared to the NMOS-only structure shown in Fig.2(b), makes the complementary structure more difficult to design with low supply voltages.

The tank inductor is a spiral structure. The component values in the simplified Pi model of the spiral inductor were taken from [9]. AC simulation of the inductor model predicts a quality factor of around 2.5 at 2GHz. It is an octagonal structure built with three metal layers of the technology, connected in series. The cross coupled negative conductance generator is to be connected to the third metal layer to minimize the capacitive coupling to the substrate. The varactor is a PMOS capacitor operating in depletion. The phase noise of the CMOS VCO is calculated based on the impulse sensitivity function, $\Gamma(\omega_\tau)$, [4], which is a dimensionless, frequency and amplitude independent function periodic in $2\tau$ that characterizes how sensitive the output phase of the oscillator is to an impulse injected into it. Note that, as the value of the impulse sensitivity function depends on at what phase, $\omega_\tau$, the impulse is injected into the oscillator, time-variability is involved into the computations. The
phase noise spectrum in the $1/f^2$ region is given by,

\[ \mathcal{L} \{ \Delta \omega \} = \sum_{n} \frac{\omega_{1/f}^2}{q_{\text{rms,n}}} \text{cos}(n \omega_{\tau}) \Delta \omega^2 \]  

(1)

where $\Delta \omega$ is the offset frequency from the carrier, $\Gamma_{\text{rms,n}}$ is the rms value of the impulse sensitivity function (ISF) of the nth noise-generating component of the oscillator, $\omega_{1/f}^2/\Delta f$ is the mean-square noise current density of the associated component and $q_{\text{rms,n}}$ is the maximum charge swing across the tank capacitance. As the impulse sensitivity function is periodic, it can be expressed as a Fourier Series

\[ \Gamma(\omega_{\tau}) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n \omega_{\tau}) \]  

(2)

where the coefficients $c_n$ are real. $c_0$, the dc coefficient of ISF, governs the upconversion of $1/f$ device noise around the carrier, whereas the other coefficients are responsible for the downconversion of white noise near the harmonics of the carrier, [4], [6]. The spectrum of phase noise in the $1/f^2$ region, where the upconversion of device $1/f$ noise around the carrier is observed is described by,

\[ \mathcal{L} \{ \Delta \omega \} = \sum_{n} \frac{\omega_{1/f}^2}{q_{\text{rms,n}}} \text{cos}(n \omega_{\tau}) \Delta \omega^2 \]  

(3)

where $\omega_{1/f}$ denotes the $1/f$ noise corner of the associated device in the oscillator. As the equations describing the spectrum of phase noise show, the ISF of all the noise-generating components should somehow be calculated to compute their contribution to the phase noise of the VCO. Once the individual contributions are computed, the phase noise of the VCO can be determined through summation as (1) and (3) suggest. Note that each $\omega_{1/f}^2/\Delta f$ in the equations represents drain current noise, resistor noise, varactor noise and inductor noise. The varactor and inductor noise are due to the finite quality factor, Q, of the components and they can easily be expressed in terms of the loss resistances of the components which can be obtained from their respective simulated Q values at the frequency of oscillation.

To determine the ISF of a noise-generating component in the VCO, an impulsive current source that represents the associated noise source was connected in parallel with the component. The resulting phase shift was measured through transient simulations, as explained in [4]. The area of the current impulse injected corresponds to the amount of charge perturbation applied to the circuit and in order for linearity, which is one of the bases of the theory, to hold, the amount of charge injected should be much smaller than the steady-state charge swing across the tank capacitance. A scaling on the measured phase shift was done after the transient simulations, accordingly. As mentioned before, the value of ISF, $\Gamma(\omega_{\tau})$, depends on at what phase, $\omega_{\tau}$, the current impulse is injected into the circuit and it is this characteristic of the ISF that accounts for the time-variance involved in the theory. In order to determine the Fourier coefficients of the ISF of a noise-generating component accurately, the number of current impulse injection simulations within an oscillation period, which corresponds to $2\pi$ radians, should be kept as high as possible. The current impulse is injected once the oscillating waveform reaches its steady-state. The simulations are repeated N times by changing the phase at which the current impulse is injected within one oscillation period with $2\pi/N$ increments each time with respect to the starting phase. Obviously, the accuracy with which (1) and (3) estimate the phase noise depends on the accuracy with which the Fourier coefficients are determined. As an approximate figure for the phase noise of the VCO was targeted for the analytical calculations, the mean-square value of the ISFs of the tank inductor and the tank varactor were taken as 1/2, as is the case for an ideal sinusoidal waveform of an LC oscillator, [4]. Furthermore, the number of transient simulations for the ISF determination of each component was kept at a relatively small number of 50.

A comparison between the analytically calculated and simulated phase noise of the CMOS VCO is plotted in Fig. 5. The calculated phase noise agrees well with the simulation result. The better matching at the $1/f^2$ spectrum of the phase noise indicates that the accuracy in the determination of the dc values of the ISFs of the components is somehow superior to the accuracy in the determination of the mean-square values of the ISFs of the components, through charge injection simulations.

![Figure 5: SpectreRF simulated vs. analytically calculated phase noise of the CMOS VCO](image)
The calculated percentage contributions at 3MHz offset show that, the low Q inductor is the main contributor to the phase noise at large offset frequencies. At low offsets from the carrier though, i.e. at 1kHz, with the addition of the upconverted flicker noise of the transistors, the percentage contributions differ considerably. The largest contributor is the NMOS cross coupled pair, while the PMOS cross coupled pair contributes much less with its superior flicker noise in the technology. By observing the symmetry properties of the oscillating waveform through the proper sizing of the cross-coupled transistors it is possible to reduce the dc values of the ISFs of the MOS transistors, which govern the upconversion of the flicker noise around the carrier, to improve the close-in phase noise, [4]. As for the phase noise at large offsets, an integrated LC tank with higher quality factor should be used.

![Figure 6: Simulated phase noise of the NMOS-only VCO @ 3MHz offset vs. the quality factor of the tank inductor](image)

A second VCO designed with only NMOS transistors in the negative-conductance generator uses the same inductor as its complementary cross coupled counterpart. The same PMOS varactors are used in the tank. The NMOS-only VCO achieves nearly the same phase noise level as the VCO with the complementary cross coupled pairs investigated above but with almost twice the power consumption. The lack of the PMOS pair prevents the optimization of the negative-conductance generator transistors for lower noise upconversion. The advantage of the NMOS-only VCO is that the circuit can operate with a lower supply of 2.5V as opposed to the 3V supply of the complementary one. As the Q of the inductor used in the tank is around 2.5 and the Q of the varactor is around 35 at the frequency of oscillation, the quality factor of the tank is determined by that of the inductor. In order to evaluate how the quality factor of the inductor affects the phase noise of the VCO at large offsets quantitatively, SpectreRF simulations were performed using the NMOS-only VCO test bench, by setting the Q of the tank inductor as a parameter. The simulation results are plotted in Fig.6, where the y-axis is the simulated phase noise at 3 MHz offset in dBc/Hz and the x-axis is the Q of the inductor. A phase noise value of around -131dBc/Hz is obtained with an inductor Q value of 10, which is a realistic Q value for optimized integrated inductors, [6]. The significant improvement in the phase noise performance as the inductor Q increases as observed in Fig.6 clearly illustrates the dominant contribution of the inductor noise in the phase noise of the VCO at large offsets.

IV. EXPERIMENTAL RESULTS

Two CMOS VCOs using only NMOS cross coupled pairs for negative-conductance generation as shown in Fig.2 were designed and fabricated with HP 0.5μm and TSMC 0.35μm CMOS technologies through MOSSIS. The chip micrograph of the VCO with HP 0.5μm CMOS is shown in Fig.7. Both VCOs were bonded to TQFP 44 packages and the measurements were taken on the packaged parts. The spiral inductors used in the VCOs are identical in geometry to the structure mentioned in the previous section.

![Figure 7: Die micrograph of the VCO with HP 0.5μm CMOS](image)

The frequency spectrum of the CMOS VCO in TSMC 0.35μm is plotted in Fig.8. The frequency of oscillation is 2.16GHz with the VCO core drawing 3.8mA from a 1.3V supply. The second and third harmonic levels are measured to be 50dB lower than the fundamental. The tuning range of the VCO shown in Fig.9 is 18%, when the VCO core is drawing 6.8mA from a 1.8V supply. The measured tuning range is reduced to around 4.8% with 1.3V. The limitation in the measured tuning range with the reduced supply voltage is observed to be due to the decreased tail current of the negative-conductance generating active devices because of the insufficient voltage headroom of the current mirror transistor. On-wafer S-parameter measurements of the PMOS inversion-mode varactor used in the VCO core yielded a $C_{max}/C_{min}$ ratio of around 2.3 at 2GHz.

The VCO designed with HP 0.5μm CMOS draws
Figure 8: Frequency spectrum of the TSMC 0.35μm CMOS VCO with Vdd=1.3V

9mA from a 2.5V supply when oscillating at 2.14GHz. Fig.10 shows the measured phase noise of the VCO with the control voltage set at 2.5V. The low quality factor of the spiral inductors in the technology used (around 2.5 at 2.2GHz) limited the phase noise to a relatively high value of -124dBc/Hz at 3 MHz offset from the carrier. The measured value is within 2dBs of the SpectreRF simulated value shown in Fig.6.

Figure 9: Measured tuning range of the TSMC 0.35μm CMOS VCO with Vdd = 1.8V

Figure 10: Phase noise of the VCO with HP 0.5μm CMOS at f osc = 2.14GHz

V. CONCLUSIONS

Negative conductance VCOs with fully integrated resonators in Si technologies show promising results as the quality of the integrated resonator passive elements are improved by the designers and process developers. Recent improvements in the phase noise theory enable the designers to correctly identify the component contributions for optimization in the design process. This paper presented the design trade-offs of negative-conductance VCO structures in CMOS and BiCMOS technologies together with experimental results of two fully integrated CMOS VCOs at 2.2GHz.

VI. REFERENCES


