A COMPARATIVE STUDY OF DIGITAL $\Sigma A$ MODULATORS FOR FRACTIONAL-N SYNTHESIS

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Abstract: This paper investigates the design of digital $\Sigma A$ modulator (SDM) for fractional-N frequency synthesis. The design considerations are presented. Characteristics of digital $\Sigma A$ modulators compared with their analog counterparts are addressed. Simulation results of 4 types of digital SDMs are presented. The pro’s and cons of each topology are discussed in detail. Design guidelines of digital SDMs for fractional-N synthesizers are given by this comparative study.

1. INTRODUCTION

Frequency synthesizers are widely used as local oscillators for frequency translation in wireless communications. The principle limitation of an integer-N frequency synthesizer is that its frequency resolution is equal to the PLL reference frequency. Fractional-N approach eliminates this limitation, but the fractional spur, is a big concern. Sigma-delta noise shaping technique is applied to fractional-N synthesis to achieve arbitrarily fine frequency resolution and suppress or eliminate the fractional spur [1]-[9].

There are various topologies for analog SDMs used in data converters. Similarly, there are different topologies of digital SDMs for synthesizers. A large number of publications on the design of analog $\Sigma A$ modulators can be found in the literature [10]-[12]. However, little attention has been paid to the design of digital ones [13]-[14]. This paper compares different digital SDMs and provides useful guidelines for architecture designers. Section 2 deals with the design consideration of digital $\Sigma A$ for fractional-N synthesizers. In section 3, different design considerations of digital SDMs in comparison with analog SDMs are pointed out. Several topologies of digital SDMs are evaluated in terms of their performances in this special application. Conclusions including an explicit comparison table are given in section 4.

2. DESIGN CONSIDERATIONS

Figure 1 shows the concept of $\Sigma A$ fractional-N synthesizer. A digital SDM is used to control the frequency division ratio in the PLL. The instantaneous division ratio is the sum of a base integer, $N_a$, and the integer output of the SDM, $n_o (t)$, so the average fractional division ratio is

$$ N = N_a + \frac{n_o (t)}{M} $$

(1)

where $n_o (t)$ is the average output of SDM, and

$$ \frac{n_o (t)}{M} = \frac{K}{M} $$

(2)

where $K$ is the input integer to the SDM, and $M$ is the modulo used in the SDM.

When the PLL reaches the steady state, its output frequency is,

$$ f_{out} = N \cdot f_{ref} = \left( N_a + \frac{K}{M} \right) \cdot f_{ref} $$

(3)

and the frequency resolution would be

$$ \Delta f = \frac{1}{M} f_{ref} $$

(4)

The SDM used in a synthesizer is to randomize the instantaneous division ratio and hence push phase noise associated with the divider from low frequencies to high frequencies. The loop filter filters out the phase noise in high frequencies. Open-loop approximation is used to map the SDM quantization noise into PLL output phase noise [2]. This approach opens the connection between the VCO and frequency divider and assumes that the input to the frequency divider is an ideal signal with exactly the desired frequency $N \cdot f_{ref}$. So the phase noise generated by the frequency divider is

$$ S_{n0} (f) = \left( \frac{\Delta f}{f} \cdot Q(f) \right)^2 $$

(5)

where $Q(f)$ is the rms spectral density of the quantization noise, and

$$ Q(f) = 2 \pi \cdot \frac{1}{12 f_{ref}^2} \left| H_{n0} (s) \right|^2, \quad z = e^{j 2 \pi f} $$

(6)

Since the phase transfer function from divider to PLL output is the same as the one from input to output, we can view $S_{n0} (f)$ as an equivalent input phase noise and use a closed-loop input-to-output phase transfer function to estimate output phase noise generated by the SDM.

$$ S_{n0} = S_{n0} (f) \cdot \left| H_{PLL} (s) \right|^2, \quad s = j 2 \pi f $$

(7)

Based on the above observations, we have the requirements for an SDM used in PLL-FS as follows:

1) As tone-free as possible
2) Stable dc input range meets particular applications
3) Output levels as low as possible to reduce noise mixed down due to nonlinearities in phase/frequency detector, charge-pump, loop-filter, and VCO [5], and also to reduce the phase...
noise introduced by phase detector and charge-pump.
4) Suitable for high frequency operation
5) As simple as possible to reduce power consumption and chip area.

3. DIGITAL MODULATOR TOPOLOGIES
SDMs are basically divided into two types: single-stage and cascaded. Digital SDMs, unlike their analog counterparts, don’t have any non-idealities, and when the modulator is stable, there is no overload problem. Cascaded digital modulators won’t suffer from mismatches and noise leakage from front stages, and multi-bit quantizers won’t suffer from any non-linearity, which doesn’t exit in the digital modulator at all. For the application to fractional-N frequency synthesis, the outputs from the digital SDM can only be taken as integers. Since the input to the digital SDM is a dc level, to avoid limit cycles in the modulators, a long bit-length input has to be used. 18-bit input with the LSB set to 1 is used in this paper.

2nd and 3rd-order ZA modulators are practically used for fractional-N synthesizers [1]-[2], [4]-[9], [13]-[14]. 4th or even higher order modulators are rarely used because it’s difficult to suppress the phase noise at higher frequencies by limited order of loop filter [3].

For 2nd-order modulators, the architecture is almost unanimously MASH 1-1 [4]. This paper concentrates on study of different topologies of 3rd-order modulators.

A. MASH 1-1-1
The MASH 1-1-1 architecture based on digital accumulators is depicted in Fig. 2 [1]. It’s very simple. The overflow from the accumulator is usually one bit, i.e., either 0 or 1, so the noise cancellation logic is of low complexity. The output has 8 levels and spreads from -3 to 4 with an average between 0 and 1. The stable input range normalized to the modulus is from 0 to 1. It’s inherently stable. This topology is suitable for pipeline operation for very high clock frequencies.

The Matlab simulation of MASH 1-1-1 topology is made to evaluate its performance. The simulation was run on 2^9 points and the clock frequency is 16.384MHz. Fig. 3 shows its output power spectrum density (PSD) and phase detector input phase error distribution. The phase error is normalized by a factor of N/(2π). We observe that the output is quite tonal and the phase error spreads widely. Although the input stable range covers from 0 to 1, input levels too close to 0 or 1 will generate high-level in-band spurs at the synthesizer output [3].

B. MASH 1-2
To reduce the number of output levels, MASH 1-2 as shown in Fig. 4 was used in [14]. The output has four levels from -1 to 2.

The simulation results are shown in Fig. 5. The spurious content of the PSD is better than MASH 1-1-1, but the spurs in high frequencies will be mixed down to low frequencies by the non-linearity of analog circuits in the PLL.

The big disadvantage of MASH 1-2 is that it only allows the input to operate about 75% of the whole fractional range [14]. This will limit its application in fractional-N frequency synthesizers.

C. Single-stage with multiple feedforward
Compared with MASH architecture, single-stage architecture has better noise shaping characteristics for dc inputs. But it is subject to instability and smaller stable input range. The latter limitation can be eliminated with a multi-bit quantizer in digital SDMs.

A modified single-loop multiple feedforward modulator used in [2] is shown in Fig. 6. Here the quantizer output is limited to three levels: 0, 1 and 2. The feedback branches can be truncated to reduce the circuit complexity, power and area. Simulation shows that the input stable range covers the whole fractional range from 0.5 to 1.5. Since the SDM output has only three levels, the phase error appearing at the phase detector input is well concentrated. A few weak tones are observed in the PSD of the modulator output.

D. Single-stage with multiple feedback
Another version of single-stage implementation considered in this paper is the multi-feedback topology shown in Fig. 8. It’s used in [9]. In this architecture, to obtain reasonable stable input range we have to set the number of quantization levels as high as nine, i.e., from -4 to 4. The bit-lengths of the adders before the accumulators are much shorter than the accumulators themselves, so the complexity of these adders is pretty low. Simulation shows that if we want to reduce the number of output levels, we have to scale the input to each accumulator and each feedback branch as indicated in [12]. In that case, the noise shaping and spurious content are much worse. Quantization noise flattens at high frequencies and noise level at low frequencies rises. The simulation results shown in Fig. 9 reveals that we get almost tone free output at the expense of large number of output levels. Compared with MASH 1-1-1, which has eight output levels, the phase detector phase error is much better concentrated.

4. CONCLUSIONS
From the simulation results of 3rd-order digital SDMs presented above, we observe that the single-stage architecture is better than the cascaded one in terms of spurious content. The more levels of the quantizer, the larger stable dc input range, better noise shaping characteristics and fewer tones. Fewer output levels are preferred in terms of non-linearity concerns and phase noise associated with phase detector and charge-pump, as stated in Section 2. So there is a tradeoff in choosing the number of output levels. Intuitively, if the basic division number N_0 is small, fewer output levels are preferred. The relationship
between digital SDM tones, nonlinearities of PLL analog parts and output fractional spurs is the topic of future research. It will provide further insight into the design of digital SDM for the fractional-N frequency synthesizer.

The table at the end of this page provides a concise comparison of the performances of the 4 types of digital SDMs discussed in section 3.

5. ACKNOWLEDGEMENT
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6. REFERENCES

Table: performance comparison of SDM's

<table>
<thead>
<tr>
<th>architecture #</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
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<tr>
<td>noise shaping</td>
<td>good</td>
<td></td>
<td>fair</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>good</td>
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<td>spurious content</td>
<td>very tonal</td>
<td>some tones</td>
<td>a few tones</td>
<td>almost tone-free</td>
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<tr>
<td>stable dc input range</td>
<td>0 ~ 1</td>
<td>0.125 ~ 0.875</td>
<td>0.263 ~ 1.678</td>
<td>-2.50 ~ 2.50</td>
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<tr>
<td>output levels</td>
<td>8 levels: -3 ~ 4</td>
<td>4 levels: -1 ~ 2</td>
<td>3 levels: 0 ~ 2</td>
<td>9 levels: 4 ~ 4</td>
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<tr>
<td>max clock frequency</td>
<td>$f_{max}$</td>
<td>$0.5f_{max}$</td>
<td>$\approx f_{max}$</td>
<td>$0.33f_{max}$</td>
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<tr>
<td>complexity / area / power</td>
<td>Almost the same, since accumulators dominate complexity / area / power and each</td>
<td>has 3 accumulators.</td>
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Fig. 1. $\Sigma\Delta$-PLL fractional-N synthesizer

Fig. 2. MASH 1-1-1 SDM

Fig. 3. Simulation of MASH 1-1-1 SDM

Fig. 4. MASH 1-2 SDM

Fig. 5. Simulation of MASH 1-2 SDM

Fig. 6. Single-stage multiple feedforward SDM

(a) PSD

(b) Normalized phase error

Fig. 7. Simulation of single-stage feedforward SDM

Fig. 8. Single-stage multiple feedback SDM

(a) PSD

(b) Normalized phase error

Fig. 9. Simulation of single-stage feedback SDM