A PROGRAMMABLE RAIL-TO-RAIL CONSTANT-"G_M" INPUT STRUCTURE FOR LV AMPLIFIER

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ABSTRACT

We proposed a novel technique for low voltage rail-to-rail constant-\(g_m\) input stages, which does not depend on the operation regions of the MOS transistors. An Op Amp was designed to demonstrate the new idea using MOSIS AMI 1.2 \(\mu\)m technology. A 2.5 MHz unity-gain bandwidth with \(61^\circ\) phase margin was achieved when driving 10 \(k\Omega\) and 10 \(pF\) load, with 240 \(\mu\)A current consumption and a power supply of 3 V. The \(g_m\) variation of the input stage is within \(\pm3\%\) from rail-to-rail. By changing the bias current, the unity-gain bandwidth could be programmed from 90 \(kHz\) to 3 MHz.

I. INTRODUCTION

Op Amp is one of the most widely used components in analog and mixed-signal environments, the design constraints of Op Amps directly affect the functionality and performance of the whole system. With a low supply voltage, we have to maximize the signal swing to keep a high enough dynamic range, which is defined as the ratio of the maximum allowable signal swing (or power) under some distortion constraints, over the noise floor. Thus rail-to-rail input and output swing is a very desirable feature in low voltage design. For the working configurations of Op Amp shown in Fig. 1, non-inverting, voltage follower, and differential to single-ended conversion configurations need some input common-mode (CM) swing for the amplifier. An input stage with rail-to-rail CM swing is necessary for an Op Amp which works as a voltage buffer as shown in Fig. 1(c).

For systems with a supply voltage higher than \(V_{TP} + V_{TN} + 4V_{DS(sat)}\), an N-P complementary input stage, in which one N-pair and one P-pair are connected in parallel, could be used to achieve a rail-to-rail input CM swing, as illustrated in Fig. 2. The problem of this simple structure is that, in the central part of the CM swing, both of N and P pairs operate, rendering a total transconductance \((g_{m,T})\) which is about twice of the value when the CM voltage is close to either of the supply rails and only the P or N pair is operating, as shown in Fig. 2. Constant transconductance \((g_m)\) rail-to-rail input stage is necessary to have an optimized frequency compensation and better linearity.

There are a number of circuit structures to achieve a constant \(g_m\), mainly including, i) Keep \(I_N + I_P\) constant [1] if the input MOS transistors work in weak inversion region, or with bipolar input stage. For MOS input stage, this scheme has the shortcoming of large area and hence a slow speed. If the transistors work in strong inversion, a \(+40\%\) \(g_m\) deviation will be introduced. ii) Keep \(\sqrt{I_P} + \sqrt{I_N}\) [2], [3] or \(\sqrt{K_{P,N}W} + \sqrt{K_{P,P}\frac{W}{T}}\) constant. These schemes depend on the quadratic characteristic of MOSFETs, which is not accurately followed by short channel transistors, and also some error is introduced due to weak inversion operation in takeover regions. iii) 4 times \(I_N\) or \(I_P\) when only one pair operates [2]. There is a \(+15\%\) systematic variation at the 2 takeover regions, and the slew rate of the amplifier changes as large as 2 times from rail-to-rail. iv) Back-up pair with current switches [5] or 6-pair structure [6]. Although the slew rate is constant, the systematic \(g_m\) variation is as large as \(+20\%\). v) Max-
imum/minimum current selection [7]. This scheme has a low \( g_m \) variation and could operate well in all of the weak, moderate and strong inversion regions of MOSFETs, with the expense of slightly complicated circuit. vi) Electronic zener [8]. This scheme has similar drawbacks as structure (ii). vii) Level shift [9]. For this scheme, \( g_m \) variation is sensitive to \( V_T \) and supply voltage changes.

In Section II and III, we will propose a new constant-\( g_m \) circuit structure for the input stage, which belongs to category (v) as summarized above, and hence has a constant \( g_m \) independent operation regions of the input transistors. By changing the bias current, the unity-gain bandwidth or GBW (Gain BandWidth product) could be programmed in a very wide range to meet different specifications of the applications. An Op Amp was designed using the proposed rail-to-rail input structure. Some simulation results are demonstrated in Section III.

II. THE NEW MINIMUM CURRENT SELECTION CIRCUIT

Our proposed constant-\( g_m \) rail-to-rail stages belongs to category (v) as summarized above in Section I (more accurately, minimum current selection), with a neat circuit structure. Interested readers are referred to [7] for detailed explanations of the working principles of constant \( g_m \) using maximum/minimum current selection scheme.

Our novel minimum current selection circuit is depicted in Fig. 3(a), where M1~M4 are transistors with the same size, and \{M5, M6\} form a 1:1 current mirror. We can derive the following equation according to the MTL (MOS Translinear Loop) [10] principle by first order approximation assuming quadratic law of MOS characteristics stands:

\[
\sqrt{I_{D1}} + \sqrt{I_{D3}} = \sqrt{I_{D2}} + \sqrt{I_{D4}}
\]  

Further assume current mirror formed by M5 and M6 is an ideal one with a unity current transfer ratio. By substituting \( I_{D1} \) (i from 1 to 4) with \( I_{D1} = I_{D4} = I_{in2} - I_{out}, I_{D2} = I_{in1}, I_{D3} = I_{out} \) we can obtain the following expression

\[
\sqrt{I_{in2} - I_{out}} + \sqrt{I_{in1}} = \sqrt{I_{in2} - I_{out}} + \sqrt{I_{out}}
\]

When \( I_{in2} > I_{out} \), the \( \sqrt{I_{in2} - I_{out}} \) term at both sides could be canceled, we could obtain \( I_{out} = I_{in1} \); or, when \( I_{in2} > I_{in1}, I_{out} = I_{in1} \). But if \( I_{in2} < I_{in1} \), the translinear loop is broken and all \( I_{in2} \) will flow through M3, so \( I_{out} = I_{in2} \). From above we could know,

\[
I_{out} = \min(I_{in1}, I_{in2})
\]

Note that the structure depicted in Fig. 3(a) does not depend on the quadratic characteristics of MOS transistors, as long as the \( I_D \sim V_{GS} \) is monotonic, which is defined as \( V_{GS} = f(I_D) \) for M1~M4. We can have the following expression,

\[
f(I_{in2} - I_{out}) + f(I_{in1}) = f(I_{in2} - I_{out}) + f(I_{out})
\]
This conclusion is confirmed by the bipolar version of this circuit as shown in Fig. 3(b). Even better minimum current selection characteristic than the CMOS implementation was achieved in HSPICE simulation.

The voltage source $V_B$ in Fig. 3(a) could be implemented as Fig. 3(c). A low impedance could result at the source of M2 due to the negative feedback loop around M2 and M7. For low frequency, the resistance at the source of M2 is given by

$$r_m = \frac{g_{m2}}{g_{m2}g_{m7}}$$

where $g_{m2}$ is the total load conductance at the drain of M2, and $g_{m2}$ and $g_{m7}$ are the transconductances of M2 and M7 respectively. M8 is added to increase the operation speed, it prevents the gate potential of M1 to drop very low when M1 and M4 are off. $V_{BN}$ and $V_{BC}$ are generated by the circuit shown in Fig. 3(d) to overcome process parameter variations and also to have a better programmability. $V_{BN}$ should have a value close to $V_T$, thus $M_{VB}$ is working in weak or moderate inversion region. But $M_{VN}$ is in strong inversion to have a high enough $V_{BN}$ to provide bias voltage for the MOS high-swing cascode circuitry.

The DC input-output characteristic of Fig. 3(c) is shown in Fig. 4 as simulated using HSPICE. An accurate minimum selection characteristic is achieved.

III. THE RAIL-TO-RAIL INPUT STAGE AND IMPLEMENTATIONS OF AN AMPLIFIER

The input stage is illustrated in the top part of Fig. 5. The bottom part of Fig. 5 is the differential to single-ended conversion and the conventional class AB output stage [11].

The HSPICE simulation results of the $g_m$ vs. $V_{L,CM}$ characteristics of the constant-$g_m$ input stage are shown in

Fig. 6(a) for $I_{TAIL} = 20 \mu A$ and Fig. 6(b) for $I_{TAIL} = 1 \mu A$. The $g_m$ variation is $\pm 5\%$ for $I_{TAIL} = 20 \mu A$ and $\pm 6\%$ for $I_{TAIL} = 1 \mu A$. Note that the $g_m$ variation in Fig. 6(b) is mostly due to the limited output resistance of the rail current transistors in saturation, not due to the minimum current selection circuit. The rail-to-rail input stage still operates when the supply voltage drops to 2.1 V for $V_{TP} = -0.9 V$ and $V_{TN} = 0.6 V$ of MOSIS AMI 1.2 $\mu m$ technology.

The frequency responses of the whole amplifier are shown in Fig. 7. The unity-gain frequency of the amplifier is 2.5 MHz for $I_{TAIL} = 20 \mu A$ and 93.5 KHz for $I_{TAIL} = 1 \mu A$, both with 10 K$\Omega$ and 10 pF load and 3V supply voltage. The GBW could be tuned from 90 KHz to 3 MHz if $I_{TAIL}$ changes from 0.9$\mu A$ to 27$\mu A$ with phase margin greater than 58$\%$ and constant-$g_m$ from rail-to-rail. The amplifier will be sent to MOSIS for fabrication, and we will present some measurement results in the future.

IV. CONCLUSIONS

A new rail-to-rail constant-$g_m$ circuit structure is proposed in this paper, which does not reply on operation regions of the input transistors. Some simulation results demonstrated that the circuit has a good constant-$g_m$ behavior from rail-to-rail input CM voltage range. The unity-gain bandwidth could be tuned in a wide range just by changing the biasing current. The amplifier will be sent to MOSIS for fabrication.

$1$ $I_{TAIL}$ is the tail current for the N and P input differential pairs.
V. REFERENCES


