A CMOS Imaging Chip for Real-Time Range Finding

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Abstract—A novel CMOS imaging chip for real-time range finding is described. The system can extract range information without any mechanical movement and all the signal processing is done on chip. All the image sensors and mixed-signal processors are integrated in a chip. A prototype chip has been fabricated in 0.5 µm CMOS technology that occupies 0.9mm x 0.9mm silicon area. It can report the distance in the range 1.5 m - 10 m in 18 scales. Analog power dissipation is 50 mW for a 5-V power supply. The paper presents the proposed range extraction concept, describes the technique and circuit architecture, and verifies functionality by simulated results.

1. INTRODUCTION

In this paper we propose a focus sensor/processor IC for real-time passive optical range-finding. Passive range-finding techniques are generally based either on disparity in stereo vision or on focus/defocus in mono vision. The latter obviously costs less but suffers either from a complex signal-processing requirement or from a need for mechanically changing lens parameters as in traditional auto-focus systems [1-3]. The technique we propose is based on a sensor plane tilted at an angle with respect to optical axis, so that it is always intersected by the image plane regardless of the distance to the object plane. A number of auto-focusing or range-finding methods based on a tilted sensor plane have already been proposed [4-8], however, they still suffer from a need for mechanical movement and/or a heavy signal-processing overhead. The proposed technique extracts range information from a single image in real time without necessitating any mechanical movement. The level of signal processing involved is so light that all processing functions are integrated with the sensor matrix on the same chip.

The proposed range-finding technique and its hardware architecture are described in Section 2. Details of circuit design and simulation results are presented in Section 3. Conclusions are given in Section 4.

II. The Proposed Range-Finding Technique and Hardware

As shown in Fig.1, the proposed range finder comprises a single lens and a sensor whose plane is tilted by an angle $\alpha$ with respect to optical axis. Also note that the sensor plane intersects optical axis precisely at the focal point F. Any object at a distance $u$ from lens projects its focused image on an image plane located at a distance $v$ behind the lens. According to Gaussian lens law, $u$ is related to $v$ by

$$\frac{1}{f} = \frac{1}{u} + \frac{1}{v}, \quad (1)$$

where $f$ is the focal length. Therefore, object distance $u$ can be calculated once the image-plane distance $v$ has been determined. Since the sensor plane is laid out at an angle, it intersects image plane for a range of $u$ values, and the position of the intersection line $l_1 l_2$ along the $w$-axis of the sensor plane depends on $u$. It is important to recognize from Fig.1 that (a) line $l_1 l_2$ is where the best focus is obtained for a given $u$, (b) this line is a projection of a line $O_1 O_2$ of the object plane, and (c) the focusable object line $O_1 O_2$ is always on the plane $x = \frac{f}{\tan \alpha}$ regardless of the value of $u$.

Therefore, the range-finder is aimed along this plane, and the closest object line on this plane projects a focused image on $l_1 l_2$. Lines of sensors laid out in parallel to $y$-axis on the tilted sensor plane continuously measure the degree of focus. We determine $v$, hence $u$, from the position $w$ of the sensor line of the highest focus.

Fig. 1. 3D and 2D view of the system
Fig. 2. Hardware architecture of a mixed-signal implementation

Shown in Fig. 2 is the hardware architecture of a mixed-signal implementation of the proposed technique. Analog output signals of all pixels in a row are evaluated by an embedded analog focus processor, which calculates the row-wise sum of the absolute value of the spatial second derivatives of pixel signals as a measure of focus. These analog focus measures are compared in a winner-take-all (WTA) block, which identifies the row of the highest cumulative second derivative, hence the highest focus. Finally, a digital distance decoder converts the index of the identified row to distance information.

III. Circuit Design and Simulation Results

The photosensor configuration adopted in the present implementation comprises a p/n-well photodiode in series with a PMOS bias transistor. This is a non-integrating continuous-time logarithmic pixel with a relatively fast response [10].

We can put the sensor lines on chip. It is just like to set the scales in the ruler. The focus processor will try to figure out which scale is well matched and report the corresponding distance, just like the way how people use ruler. The resolution of the ruler relies on the distance of neighboring scales, so is our system. The distance between the neighboring sensor lines will decide the range resolution, which depends on the size of photosensor and processor unit and the CMOS technology.

As mentioned in Section 2, each line is equipped with a focus processor to calculate the degree of focus along that line. Shown in Fig. 3 is the circuit schematic of a 3-pixel slice of the focus processor comprising pixels i-1, i, and i+1. Note that each photodiode drives a pair of NMOS transistors with a common drain. The common-drain current \( I_i \) of pixel-i can be expressed as

\[
I_i = I_B - \frac{g_m}{2} \left[ (V_{i+1} - V_i) - (V_i - V_{i-1}) \right],
\]

where, \( g_m \) represents MOSFET transconductance. The difference between \( I_B \) and \( I_i \), which approximates the second spatial derivative

\[
\Delta I_i = I_B - I_i = \frac{g_m}{2} \left[ (V_{i+1} - V_i) - (V_i - V_{i-1}) \right], \tag{2}
\]

flows out of pixel-i onto bus-i if the second derivative is positive, and out of bus-i into pixel-i if the second derivative is negative. These two busses are kept at virtually constant voltages by two opamps per row, and their currents are summed up to generate the sum of the absolute value of the second derivatives. Also note that the diodes shown in Fig. 4 are realized with diode-connected MOSFET's on the actual test chip. The simulated transfer function of a slice of focus processor, as represented by (2), is shown in Fig. 4.

The measurement of focus is represent by sum of modified Laplacian (SML):

\[
SML = \sum_{i=1}^{m-1} |\Delta I_i|.
\]

The output current of focus processor, which is the sum of bus-1 and bus-2 currents, represents an analog focus measure for each line. The current summer is shown in Fig. 5. These currents are fed into a current-based winner-take-all circuit of the well-known Lazzaro configuration [11]. This circuit selects the line of the highest output current. Finally, a digital decoder translates the index of the line of highest focus into a digital word that represents range information in terms of object distance.

To test the proposed range-finding technique and its hardware architecture, we designed a system chip in AMI 0.5\( \mu \)m CMOS technology. The photosensor matrix contains 18 lines of 16 pixels each. Each processor unit occupies 40\( \mu \)m x 40\( \mu \)m area with a fill factor 25%. The chip layout, which fits into a MOSIS tiny frame, is shown in Fig. 6. Table 1 summarizes the properties of the prototype.

Shown in Fig. 6 are the system-level simulation results. The checkerboard object pattern that is projected onto the tilted sensor plane is depicted in Fig. 7(a). The light-intensity distribution on the sensor plane for an object distance of 5m is shown in Fig. 7(b). Note how focus rapidly deteriorates along w on both sides of the line of best focus. Finally, in Fig. 7(c) the output current of each of the 18 focus processors is given for three different object distances, 2m, 6m and 10m. Indeed, the maximum current in all three cases belongs to the sensor line that corresponds to correct distance.
Table 1: Properties of the prototype system

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Focal length (lens)</td>
<td>3.86 cm</td>
</tr>
<tr>
<td>Aperture (lens)</td>
<td>3.1 cm</td>
</tr>
<tr>
<td>Range of distance covered</td>
<td>1.5-10 m (divided into 18 discrete distance levels)</td>
</tr>
<tr>
<td>Lowest illumination</td>
<td>1 lux</td>
</tr>
<tr>
<td>Power consumption</td>
<td>50mW</td>
</tr>
<tr>
<td>Technology</td>
<td>AMS 0.5 um</td>
</tr>
<tr>
<td>Power supply</td>
<td>5 V</td>
</tr>
<tr>
<td>Chip size</td>
<td>0.9 x 0.9 mm²</td>
</tr>
</tbody>
</table>

Fig. 3. A 3-pixel slice of the focus processor.

DC Response

![Graph showing DC response](image)

Fig. 4. DC response of a slice of focus processor. SML represents the spatial second-derivative.

Fig. 5. Current summer

Fig. 6. The layout of the prototype chip
IV. Conclusions

A novel range-finding technique based on passive imaging with a single camera is proposed. The technique requires a very light signal-processing overhead, and can be implemented on a single mixed-signal CMOS chip including the photosensor matrix. Simulated results on the prototype design verify real-time operation limited only by the speed of phototransduction.

REFERENCES:


Fig.7. System-level simulation results. (a) The brightness of checkerboard object. (b) Light intensity distribution in the tilted sensor plane. (c) Output current of 18 sensor lines for u=2m, u=6m and u=10m