# Agilent N8241A/N8242A
# Arbitrary Waveform Generators

## User's Guide

Agilent Technologies

**Manufacturing Part Number: N8241-90001**

**Printed in USA**

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# Notices

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The following safety symbols are used throughout this manual. Familiarize yourself with the symbols and their meaning before operating this instrument.

**WARNING** — ***Warning*** **denotes a hazard. It calls attention to a procedure which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a warning note until the indicated conditions are fully understood and met.**

**CAUTION** — *Caution* denotes a hazard. It calls attention to a procedure that, if not correctly performed or adhered to, could result in damage to or destruction of the instrument. Do not proceed beyond a caution sign until the indicated conditions are fully understood and met.

**NOTE** — *Note* calls out special information for the user's attention. It provides operational information or additional instructions of which the user should be aware.

## General Safety Information

The following general safety precautions must be observed during all phases of operation. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Agilent Technologies assumes no liability for the customer's failure to comply with these requirements.

**WARNING** **This is a Safety Class 1 Product (provided with a protective earthing ground incorporated in the power cord). The mains plug shall only be inserted in a socket outlet provided with a protected earth contact. Any interruption of the protective conductor inside or outside of the product is likely to make the product dangerous. Intentional interruption is prohibited.**

**CAUTION** This product is designed for use in Installation Category II and Pollution Degree 2 per IEC 61010 Second Edition and 664 respectively.

**WARNING** **If this product is not used as specified, the protection provided by the equipment could be impaired. This product must be used in a normal condition (in which all means for protection are intact) only.**

**WARNING** **No operator serviceable parts inside. Refer servicing to qualified personnel. to prevent electrical shock do not remove covers.**

**CAUTION** The Mains wiring and connectors shall be compatible with the connector used in the premise electrical system. Failure to ensure adequate earth grounding by not using the correct components may cause product damage, and serious injury.

# Safety Symbols

The following symbols on the instrument and in the manual indicate precautions which must be taken to maintain safe operation of the instrument.

| | |
|---|---|
|  | The Instruction Documentation Symbol. The product is marked with this symbol when it is necessary for the user to refer to the instructions in the supplied documentation. |
|  | This symbol indicates the position of the operating switch for ‘On’ mode |

| | |
|---|---|
|  | This symbol indicates the position of the operating switch for ‘Stand-by’ mode. Note, the instrument is NOT isolated from the mains when the switch is in this position.<br><br>To isolate the instrument, the mains coupler (mains input cord) should be removed from the power supply. |
|  | This symbol indicates separate collection for electrical and electronic equipment, mandated under EU law as of August 13, 2005. All electric and electronic equipment are required to be separated from normal waste for disposal (Reference WEEE Directive, 200/96/EC). |
|  | The CE mark shows that the product complies with all relevant European Legal Directives. |
|  | The C-Tick mark is a registered trademark of the Australian Communications Authority. This signifies compliance with the Australian EMC Framework Regulations under the terms of the Radio communications Act of 1992. |
| **ISM 1-A** | This is a symbol of an Industrial, Scientific, and Medical Group 1 Class A product. |
| **ICES/NMB-001** | This ISM device complies with Canadian ICES-001.<br><br>Cet appareil ISM est conforme à la norme NMB-001 du Canada. |
|  | The CSA mark is a registered trademark of the Canadian Standards Association, and indicates compliance to the standards laid out by them. |

## Trademark Acknowledgement

Microsoft® is a US registered trademark of Microsoft Corp.

MATLAB® is a U.S. registered trademark of The Math Works, Inc.

## Updated Information

Where to Find the Latest Information

Documentation is updated periodically. For the latest information about the N8241A Arbitrary Waveform Generator, including firmware upgrades and application information, please visit the following Internet URL:

http://www.agilent.com/find/synthetic

## Compliance

This product has been designed and tested in accordance with accepted industry standards, and has been supplied in a safe condition. The documentation contains information and warnings that must be followed by the user to ensure safe operation and to maintain the product in a safe condition.

## Declaration of Conformity

The Declaration of Conformity (DOC) is on file. If a copy is required, please contact an Agilent Sales Representative or the closest Agilent Sales Office. Alternately, contact Agilent at:

http://www.agilent.com/find/

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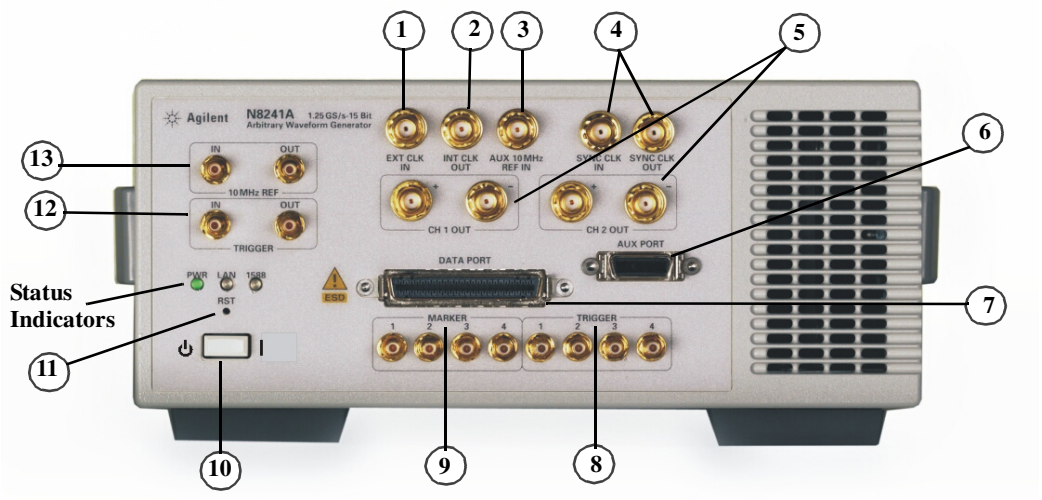
# 1 Introducing the N8241/2A AWGs

The N8241A and N8242A are wideband arbitrary waveform generators (AWGs) capable of creating high-resolution waveforms for radar, satellite and frequency agile communication systems. Each channel of the AWGs operates at 1.25 GSa/s. The N8241A features 15 bits of vertical resolution and the N8242A 10 bits. Both AWGs offer dual differential output channels to drive both single-ended and balanced designs.

The AWGs include a complete software suite to speed waveform development and system integration supporting MATLAB®, LABVIEW, and IVI-C programmatic interfaces.

# Front Panel Interface

**Figure 1-1 N8241/2A Front Panel**




| Item | | Description |
|---|---|---|
| # | Name | |
| 1 | **EXT CLK IN** | Use this 50 ohm SMA connector to input an external sample clock. It will accept clock rates in the range of 100 MS/s through 1.25 GS/s. Refer to "External Clock" on page 69 for more information. |
| 2 | **INT CLK OUT** | Use this 50 ohm SMA connector to route the internal 1.25 GS/s clock to other test instrument or devices. |
| 3 | **AUX 10 MHz REF IN** | This auxiliary 50 ohm SMA connector can be used to input an external 10 MHz reference. |
| 4 | **SYNC CLK IN / SYNC CLK OUT** | These connectors support synchronization of multiple modules. Refer to "Multiple Module Synchronization" on page 87. |

| Item | | Description |
|---|---|---|
| # | Name | |
| 5 | **CH 1/CH2 Out** | The CH 1 OUT and CH 2 OUT positive (+) connectors are used for single-ended operation. Use both the positive (+) and negative (-) connectors for differential operation. Refer to "Signal Conditioning" on page 84 for more information. |
| 6 | **AUX PORT** | The AUX port is reserved for future applications. |
| 7 | **DATA PORT** | The data port is reserved for future applications. |
| 8 | **TRIGGERS 1/2/3/4** | There are four SMB female trigger input connectors that are used to control the waveforms in the sequencer and create event-based signal simulation. The connectors support TTL/CMOS, ECL, and PECL logic levels. |
| 9 | **MARKERS 1/2/3/4** | There are four SMB female marker output connectors that can be used for triggering or system synchronization. The connectors are 3.3V TTL/CMOS 30 ohm series terminated. The output is capable of driving a 50 ohm load. |
| 10 | **Power Switch** | The power switch is toggled to either the ON or STANDBY position. |

| Item | | Description |
|---|---|---|
| # | Name | |
| 11 | **Reset** | The “RST” button enables you to put the LAN configuration of the instrument into a known state.<br>When you press this button the following settings are made and the system reboots:<br>• IP Address is set to 192.168.EE.FF, where EE and FF are the last two parts of the MAC address (AA.BB.CC.DD.EE.FF). This is designed to prevent multiple instruments from using the same default IP address.<br>• Subnet Mask is set to 255.255.0.0<br>• DHCP is set to ON<br>• Auto IP is set to ON<br>• The instrument hostname is set to A-N82XXA-NNNNN, where N82XXA is the instrument model number (such as N8241A) and NNNNN represents the last five digits of the instrument serial number. |
| 12 | **TRIGGER IN/OUT** | These SMB trigger input and output connectors are used to control the waveforms and create event-based signal simulation. The connectors support LVTTL logic levels and are functionally equivalent to Triggers/Markers 1-4, but have additional latency. |
| 13 | **10 MHz REF IN/OUT** | These SMB connectors can be used to input and output a 10 MHz reference. |

## Status Indicators

### PWR

The power indicator has the following states:

| State | Power Status | Illumination |
|---|---|---|
| OFF | No Power | None |
| STANDBY | Standby Power | Solid Amber |
| ON | Power is on | Solid Green |

### LAN

The LAN indicator has the following states:

| State | LAN Status | Illumination |
|---|---|---|
| ON | Normal Operation | Solid Green |
| ON | Device Identity:<br>–Needs initialization, refer to "Initializing the LAN Configuration" on page 93 | Blinking Green |
| OFF | LAN Error/Fault:<br>–No valid or duplicate IPaddress<br>–Unable to renew previously obtained DHCP lease<br>–Disconnected LAN cable | Solid Red |
| OFF | This is the state when:<br>–The system is initializing<br>or<br>–A LAN reset has been initialized | None |

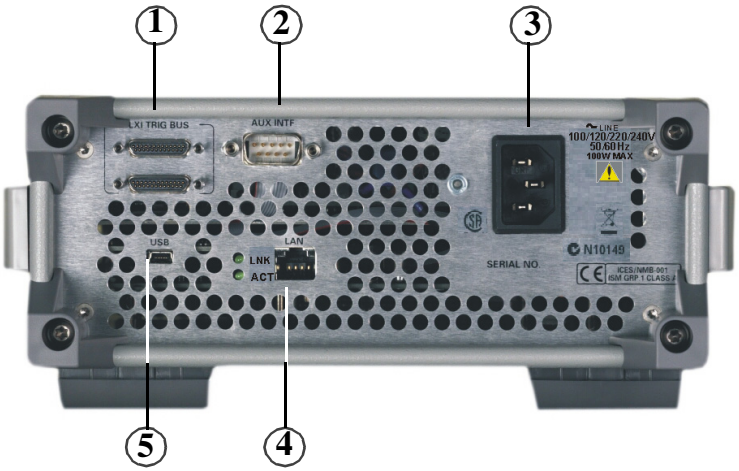
### 1588

The IEEE 1588 Clock Status has the following states:

| State | Clock Status | Illumination |
|---|---|---|
| OFF | Not synchronized | None |
| ON | Synchronized, clock is IEEE 1588 Slave | Solid Green |
| ON | Synchronized, clock is IEEE 1588 Master | Blinking Green (once every second) |
| ON | Synchronized, clock is IEEE 1588 Grand Master | Blinking Green (once every two seconds) |
| OFF | IEEE 1588 is in a fault state | Solid Red |

# Rear Panel Interface

**Figure 1-2 N8241A Rear Panel**




| Item | | Description |
|---|---|---|
| # | Name | |
| 1 | **LXI TRIG BUS** | This interface enables the instrument to detect any LXI trigger bus events or LXI LAN-based events and can output such events.<br><br>Inbound events control the arming and triggering of the instrument subsystem for performing measurements and other operations. Outbound events are used to notify other LXI devices of specific conditions.<br><br>An LXI TRIG BUS cable and terminators will be available from Circuit Assembly in the near future. |
| 2 | **AUX INTF** | This 9-pin serial interface connector is for factory-use only. |
| 3 | **AC Power Receptacle** | The AC voltage is connected here. The power cord receptacle accepts a three-prong power cable that is shipped with the instrument. The voltage range is 100/120/220/240 volts with a frequency range of 50 to 60 Hz and is automatically selected by the power supply. |

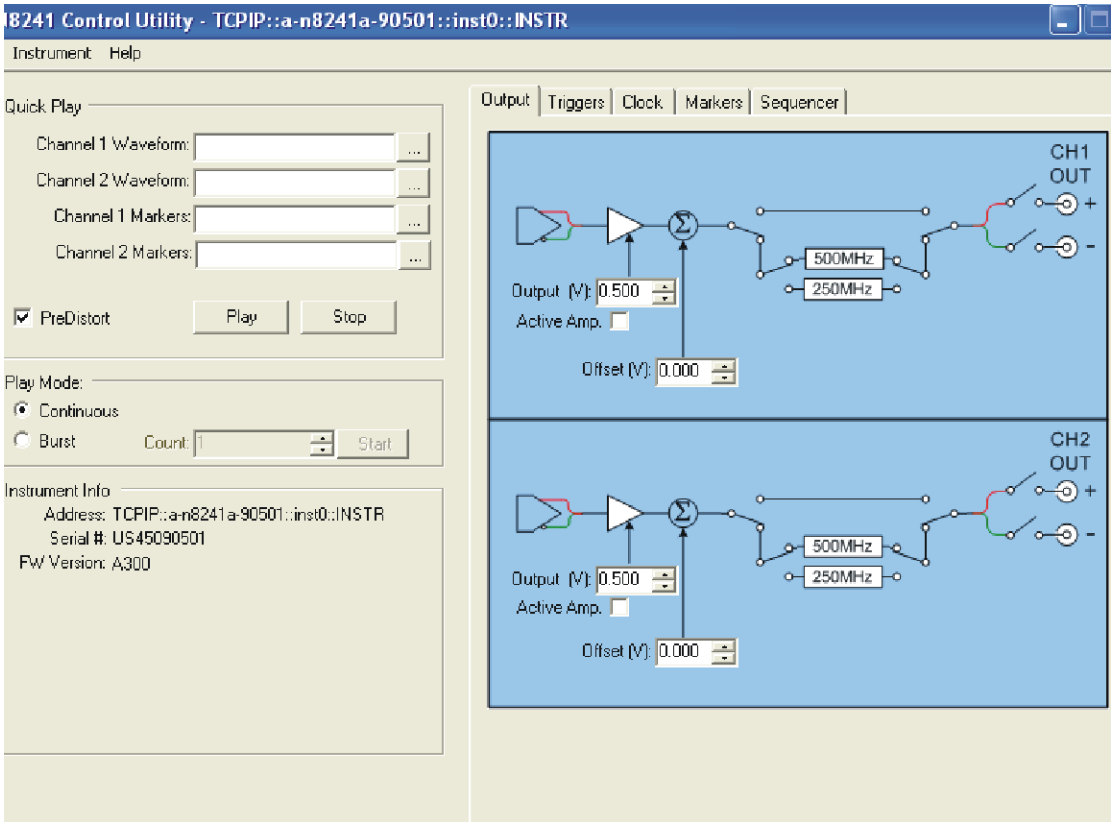
| Item | | Description |
|---|---|---|
| # | Name | |
| 4 | LAN | This local area network (LAN) interface allows communication through a 100BaseT LAN cable. |
| 5 | USB | The USB port is reserved for future applications. |

Electrostatic discharge (ESD) can damage the highly sensitive components in your instrument. ESD damage is most likely to occur as the instrument is being installed or when cables are connected or disconnected. Protect the circuits from ESD damage by wearing a grounding strap that provides a high resistance path to ground. Alternatively, ground yourself to discharge any static charge built-up by touching the outer shell of any grounded instrument chassis before touching the port connectors.

# Graphical User Interface (GUI)

The tab-based graphical interaction of the GUI gives instant access to the AWG parameters, making it easy to configure signal output. Each tab is labeled with its contents, enabling quick access to all functions. Figure 1-3 displays the first level of the GUI. For more information on the GUI, refer to the N8241A Online Help. Access this from the application Help menu, or in Windows:
**Start > Programs > Agilent > N8241A > Help.**

**Figure 1-3 N8241A Control Utility**



# Getting Started

## System Requirements

### Hardware

- Personal computer (PC) with LAN capability
- Agilent E4440A Spectrum Analyzer or equivalent (system verification)

### Supported Operating Systems

- Windows® 2000, Service Pack 4.0 or later
- Windows® XP, Service Pack 2.0 or later

### Required Software

- Windows.NET® Framework, Version 1.1 Redistributable Package, Service Pack 1 or later (included on the N8241A CD)
- IVI Compliance Package Version 2.3 or greater, which includes the IVI Shared Components (download from www.ni.com)
- Agilent IO Libraries Suite 14.1 or greater with Patch 2 (download from www.agilent.com)

## N8241/2A Installation

### Installing the Instrument

1. Plug the AWG module into the mains power supply.

**NOTE** Install the instrument so that the detachable power cord is readily identifiable and is easily reached by the operator. The detachable power cord is the instrument disconnecting device. It disconnects the mains circuits from the mains supply before other parts of the instrument. The front panel switch is only a standby switch and is not a LINE switch. Alternatively, an externally installed switch or circuit breaker (which is readily identifiable and is easily reached by the operator) may be used as a disconnecting device.

2. Connect the AWG module to a LAN line.

**Installing the Software**

Connect a LAN line to the PC and turn the PC on.

3. Download the IVI Compliance Package, which contains the IVI Engine and the IVI Shared Components.
   Go to: http://www.ni.com/
   Search on **ivi compliance package version 2.3**.
   Select **IVI Compliance Package Version 2.3 for Windows 2000//NT/XP-HWDRIVER-Support-National**

   Follow the instructions for the Download Process at the bottom of the page.
4. Download the Agilent IO Libraries Suite 14.1 with Patch 2.
   Go to:http://www.agilent.com/find/iolib
5. Insert the N8241A CD into the CD drive on your PC and follow the instructions.

**CAUTION** Before switching on this instrument, make sure the supply voltage is in the specified range.

6. Toggle the front panel switch to turn on the AWG module.

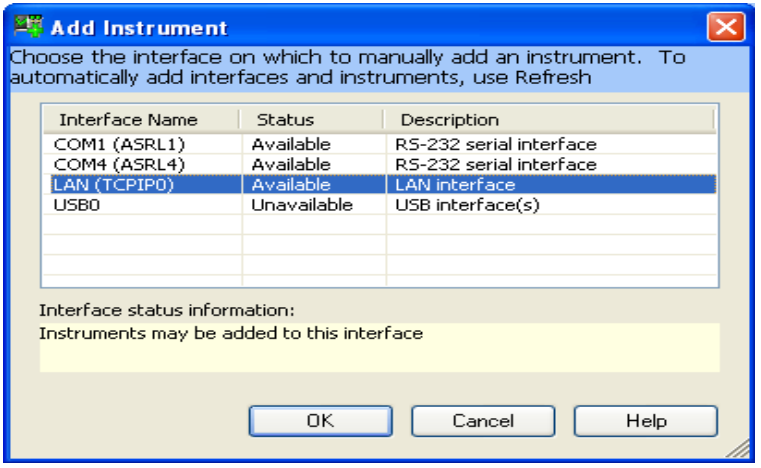
### Connecting to the AWG over the LAN

1. Open the **Agilent Connection Expert** (double-click the icon).

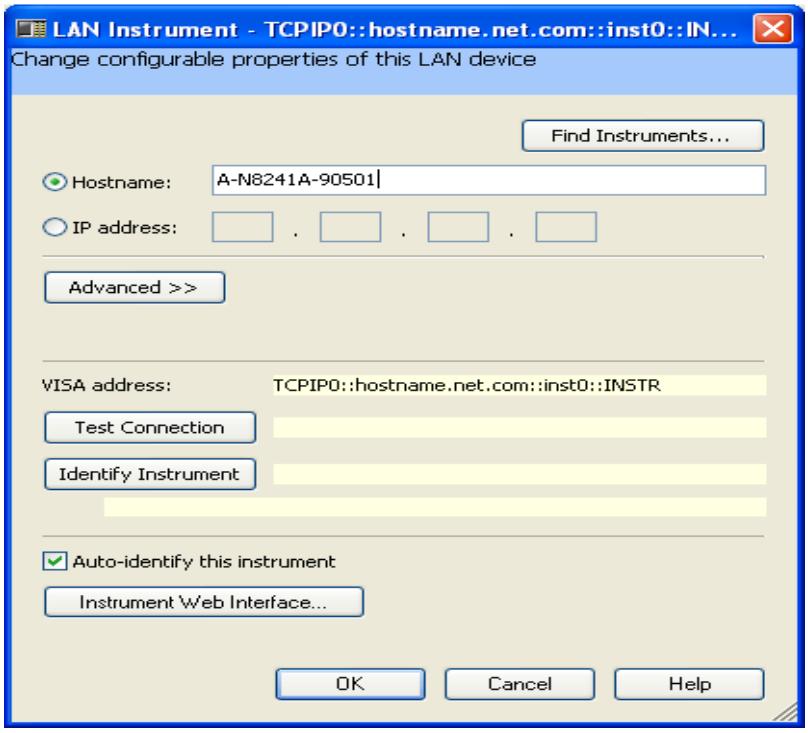
**NOTE** The Agilent Connection Expert will work only if Agilent VISA is operating as the primary VISA driver. If it is operating as the secondary driver, and another VISA such as NI VISA is the primary, you will need to add the N8241/2A using the tools of the primary VISA. The Agilent IO Libraries will alert you to this condition.


2. From the menu bar, select **Add Instrument**.


3. In the Add Instrument secondary window, select **LAN (TCPIP0) > OK**.

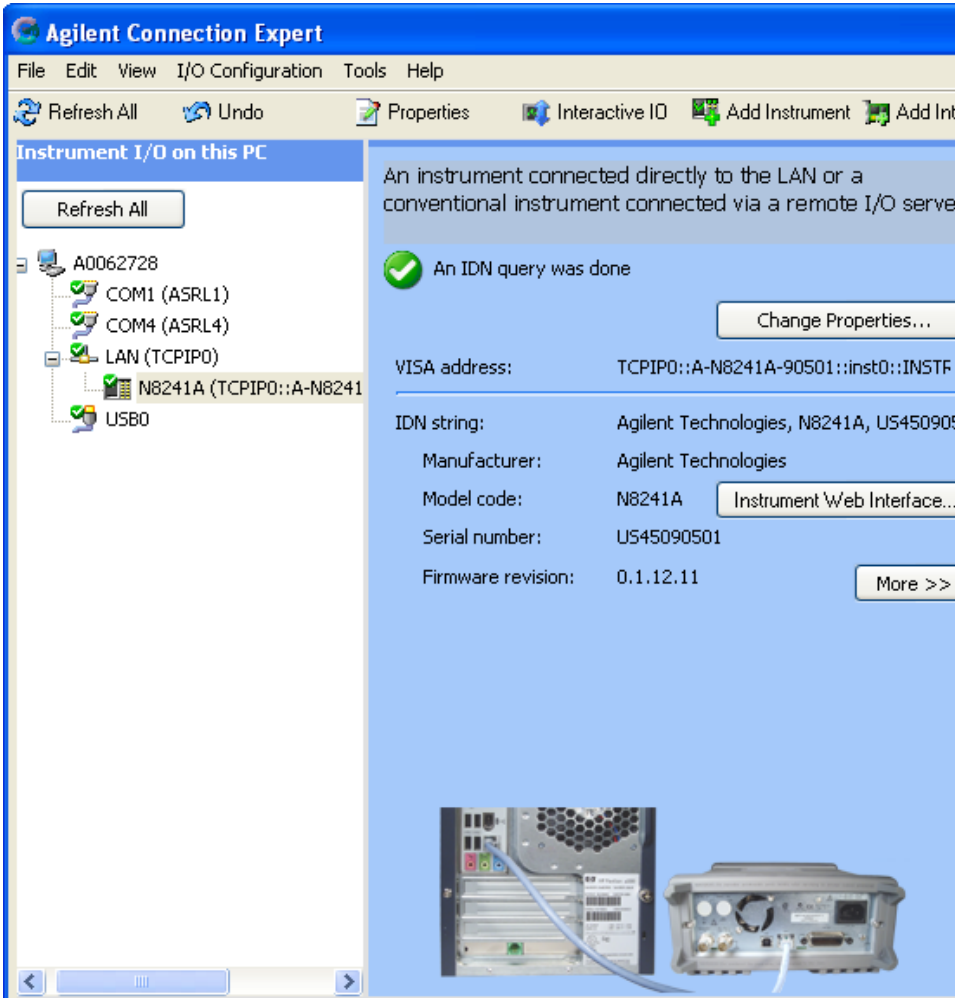


4. Enter the host name of the AWG in the **LAN Instrument** secondary window.




5. Click **OK**.

6. The AWG is now configured to the PC.



# Verifying System Operation

Prior to verifying system operation, the N8241A software must be installed on the PC and the LAN line connected to the PC and AWG module. For more information refer to "Installing the Software" on page 25 and "Connecting to the AWG over the LAN" on page 26.



## System Set Up

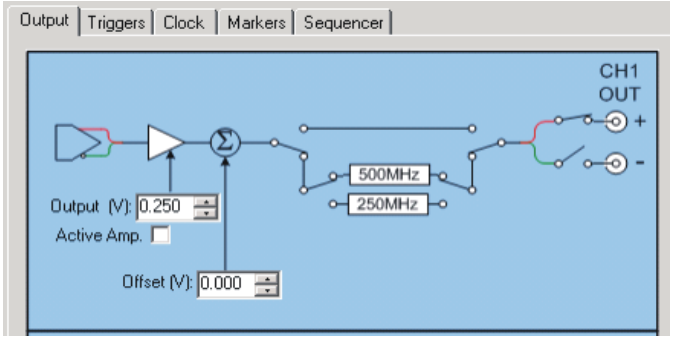
1. Connect the power cord to the AWG module and turn the power on.

**CAUTION** Before switching on this instrument, make sure the supply voltage is in the specified range.

## Waveform Generation

**NOTE** An Agilent E4440A Spectrum Analyzer or equivalent is required to view the waveforms.

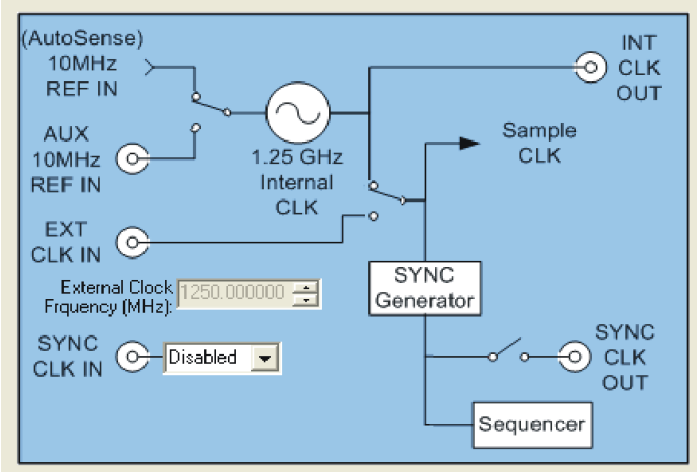
1. Connect the channel 1 positive (+) output to the spectrum analyzer RF input connector.
2. Open the user interface by double-clicking the **N8241A Control Utility** icon placed on the desktop during installation.
3. In the **Output** tab, configure the signal conditioning path to include the 500MHz reconstruction filter through **CH1 OUT** (toggle the switches you want to connect) on channel 1 and **CH2 OUT** on channel 2. The connection will automatically enable differential mode.



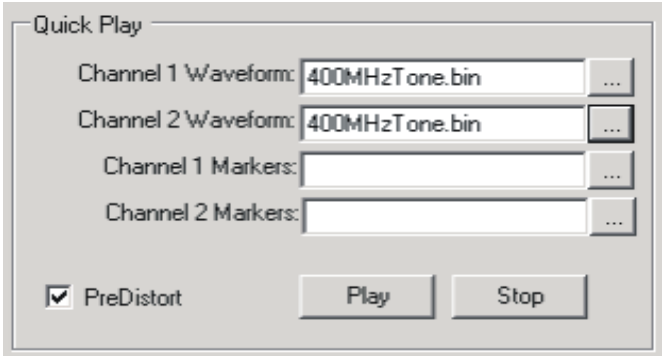

4. Click on the negative (-) node to enable single-ended mode. Notice that the

Output drops to 0.250 volts.

5. Select the **Clock** tab and confirm that the **(AutoSense) 10MHz REF IN** is configured correctly. In the **Quick Play** section of the user interface,




browse and select the **400MHzTone.bin** waveform file found on the CD for channel 1 and 2




6. Click **Play**. The spectrum analyzer cabled to channel 1 should display a spurious free dynamic range (SFDR) of at least -65 dBc for the N8241A as shown in Figure 1-4, and a SFDR of at least -50 dBc for the N8242A, Figure 1-5.

**Figure 1-4** N8241A Playback of a 400 MHz Tone

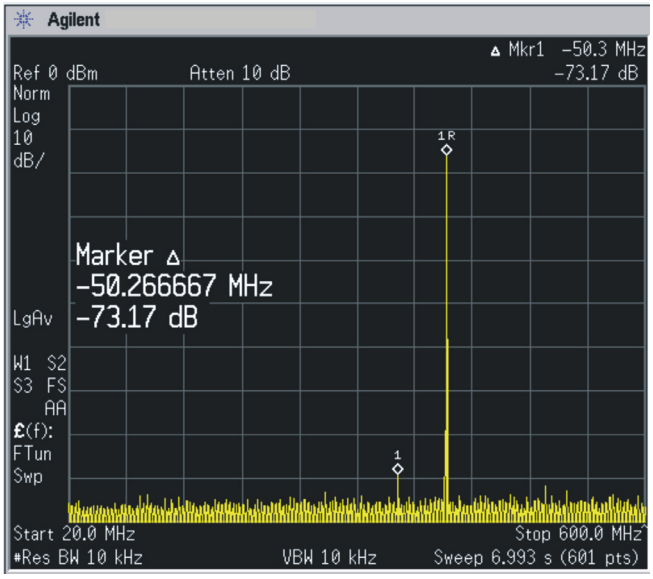
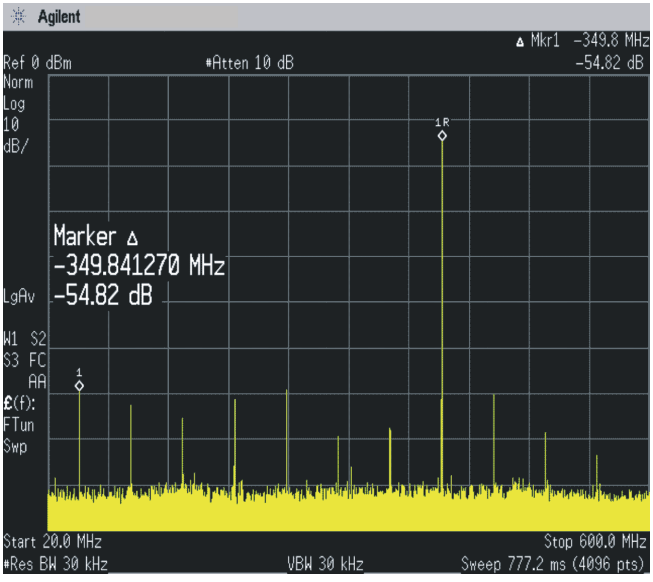



**Figure 1-5** N8242A Playback of a 400 MHz Tone




7. You should get the same performance when you connect channel 2 positive (+) to the spectrum analyzer RF input connector.

# Shutting Down the System

1. Close the N8241A Control Utility.
2. Toggle the front panel switch to place the AWG module in standby mode.

# Maintenance

## Cleaning the Instrument

To prevent electrical shock, disconnect the instrument and/or system from mains before cleaning. Use a dry cloth or one slightly dampened with water to clean the external case parts. Do not attempt to clean internally.

## Cleaning Connectors

Cleaning connectors with alcohol shall only be done with the instruments power cord removed, and in a well-ventilated area. Allow all residual alcohol moisture to evaporate, and the fumes to dissipate prior to energizing the instrument.

**WARNING**

**Keep isopropyl alcohol away from heat, sparks, and flame. Store in a tightly closed container. It is extremely flammable. In case of fire, use alcohol foam, dry chemical, or carbon dioxide; water may be ineffective.**

**Use Isopropyl alcohol with adequate ventilation and avoid contact with eyes, skin, and clothing. It causes skin irritation, may cause eye damage, and is harmful if swallowed or inhaled. It may be harmful if absorbed through the skin. Wash thoroughly after handling.**

**In case of spill, soak up with sand or earth. Flush spill area with water.**

**Dispose of isopropyl alcohol in accordance with all applicable federal, state, and local environmental regulation.**

# 2 Basic Operation

This chapter guides you through the basic operation of the AWG. Prior to following these procedures, the N8241A software must be installed on the PC. Refer to "System Set Up" on page 29 for complete instructions on how to complete this task.

# Using the Graphical User Interface

## Generating a Single Tone Signal

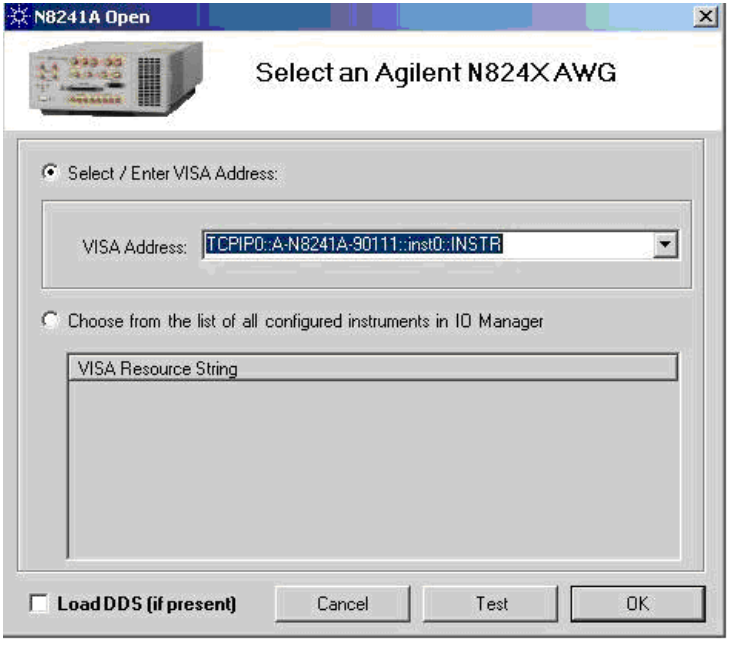
Use the following procedure as a guide to basic single-ended waveform playback with the N8241A or N8242A AWG. All waveform parameters need to be set prior to waveform playback.

**NOTE** A spectrum analyzer is required to display the waveforms.

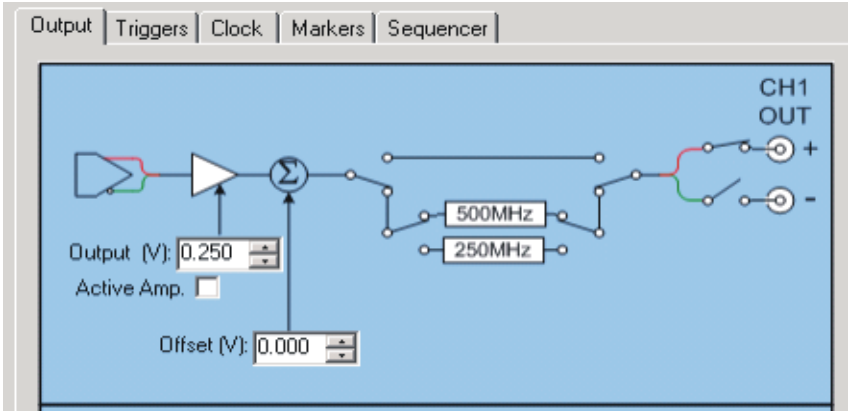
1. Connect the channel 1 positive (+) output to the spectrum analyzer RF input connector.
2. Open the user interface by double-clicking the N8241A icon placed on the desktop during installation.

**NOTE** If an icon was not placed on the desktop, go to:
**Start > Programs > Agilent > N8241A > Control Utility**

3. In the N8241A Open dialog, enter the VISA address and click **OK**.



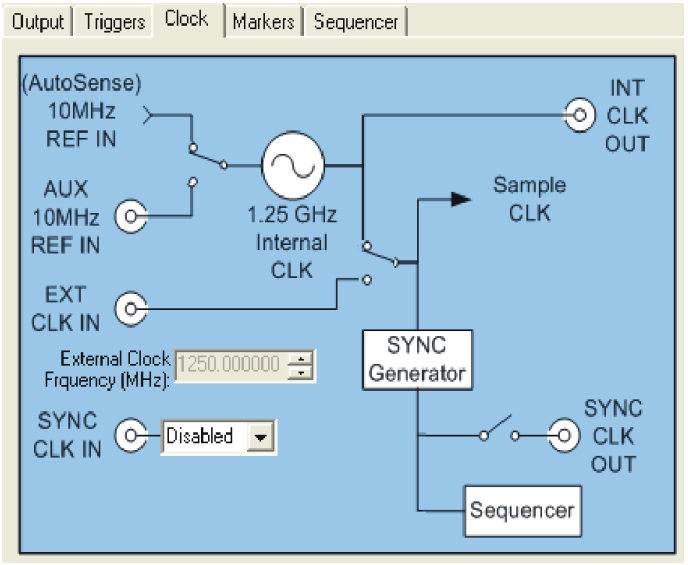
4. To select the DDS option 330 (lower-left corner of the display), refer to "Selecting the DDS Option" on page 99
5. Select the Output tab and connect a single-ended signal conditioning path to CH1 OUT (+) (click on the node that you want to connect)




The connection will automatically enable differential mode. Click on the negative (-) node to enable single-ended mode. Notice that the default gain value was 0.500 volts. Once you select single-ended mode, the value drops to 0.250 volts. These are maximum values for the modes indicated.

6. Select the **Clock** tab and confirm that the **(AutoSense) 10MHz REF IN** is

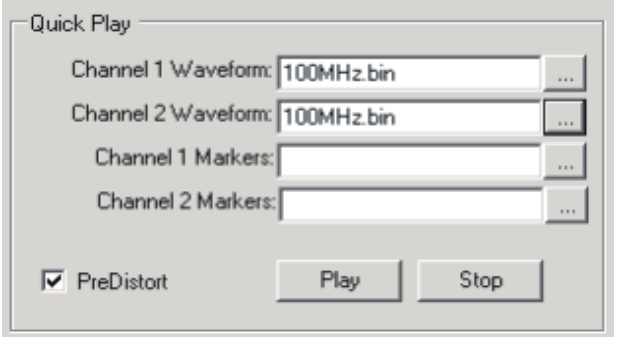
configured correctly.




7. In the Quick Play section of the user interface, browse and select the desired single-tone waveform file for Channel 1 Waveform. The AWG accepts data formatted as 16-bit signed integers ignoring the LSB.

**NOTE** Different waveforms can be loaded into channel 1 and 2, but the length of the waveforms must be the same.

8. Use the default setting for the play mode and predistortion.




9. Click **Play**.

Figure 2-1 and Figure 2-2 display a 100 MHz waveform played back on the N8241A and N8242A respectively. The SFDR is greater than –70.0 dBc for the

N8241A and greater than –50.0 dBc for the N8242A.

**Figure 2-1 N8241A Playback of a 100 MHz Tone**

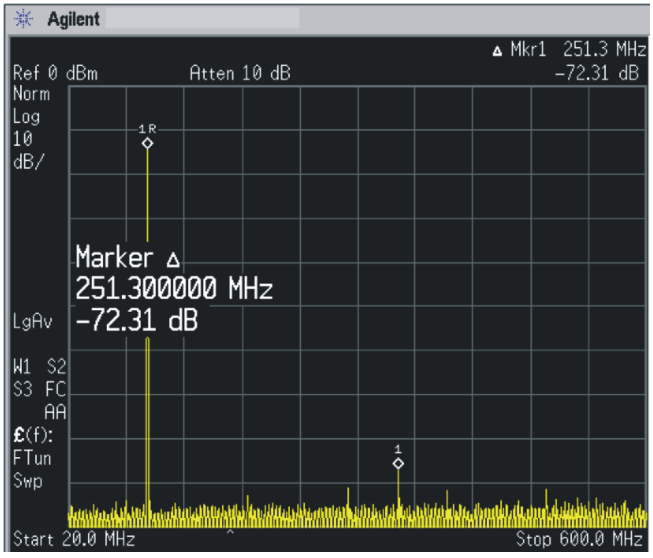
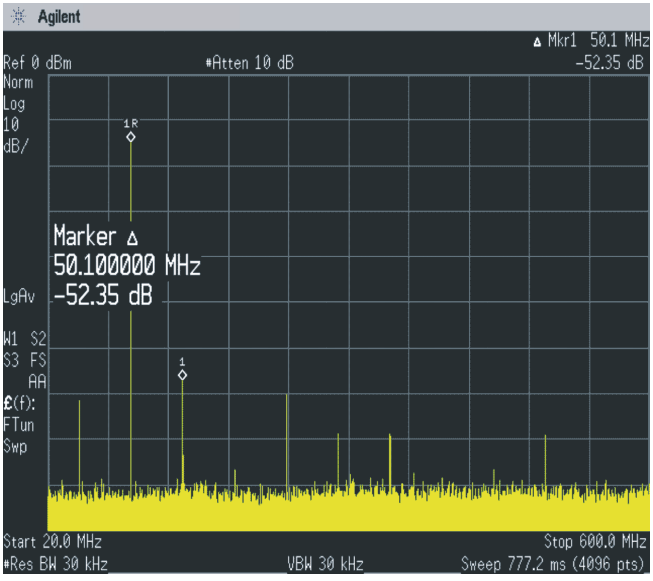
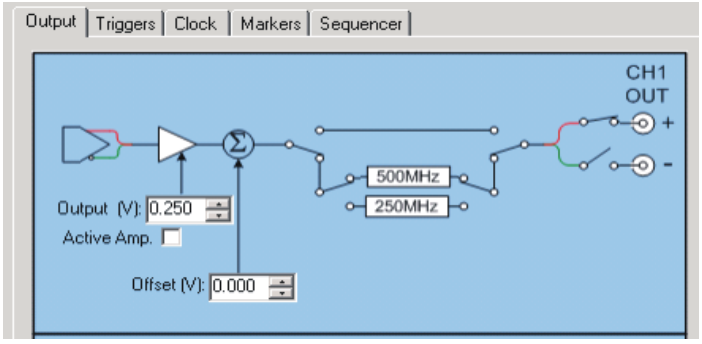



**Figure 2-2 N8242A Playback of a 100 MHz Tone**



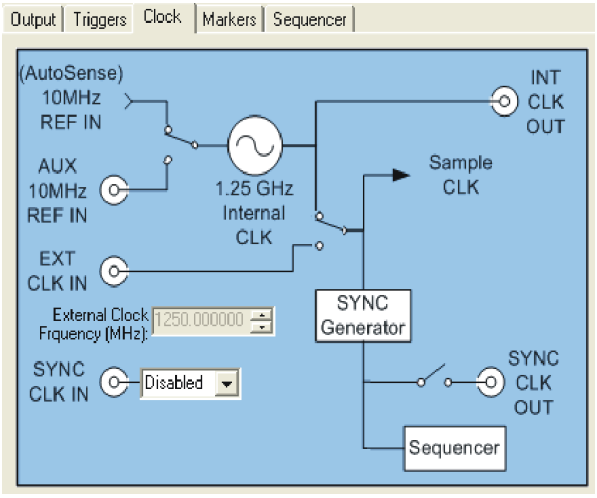
## Generating a Multi-tone Signal

1. Connect the channel 1 positive (+) output to the spectrum analyzer RF input connector.
2. Open the user interface by double-clicking the **N8241A** icon placed on the desktop during installation.
3. Select the **Output** tab and connect a single-ended signal conditioning path to **CH1 OUT** (+) (click on the node that you want to connect).

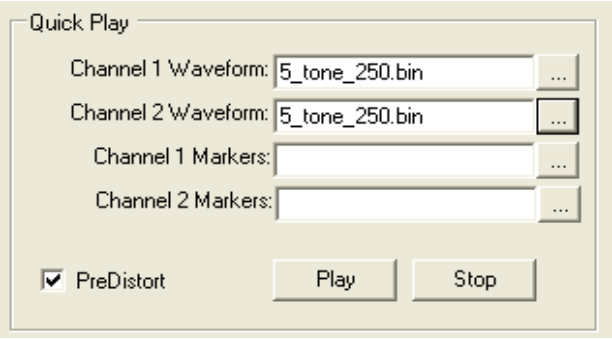



The connection will automatically enable differential mode. Click on the negative (-) node to enable single-ended mode. Notice that the default gain value was 0.500 volts. Once you select single-ended mode, the value drops to 0.250 volts. These are maximum values for the modes indicated.

4. Select the **Clock** tab and confirm that the **(AutoSense) 10MHz REF IN** is configured correctly.



5. In the **Quick Play** section of the user interface, browse and select the desired multi-tone waveform file for **Channel 1 Waveform**.
   The AWG accepts data formatted as 16-bit signed integers ignoring the LSB.




**NOTE**

Different waveforms can be loaded into channel 1 and 2, but the length of the waveforms must be the same.

6. Use the default setting for the **Play Mode** and **Predistortion**.
7. Click **Play**.

For this example, a waveform with five tones was used. The intermodulation distortion produced by the five tones played back on the N8241A is less than –60.0 dBc, Figure 2-3, and less than –45.0 dBc on the N8242A, Figure 2-3.

Although the harmonic distortion for the N8241A and N8242A is specified to be <–65 dBc and <–50 dBc respectively below the total power, the tone power is determined by the following formula:

Tone Power = Total Power – 10 log 10 (1/N)
where N= number of tones

Five tones reduces the tone power by approximately 7 dB.

**Figure 2-3 N8241A Playback of Five Tones**

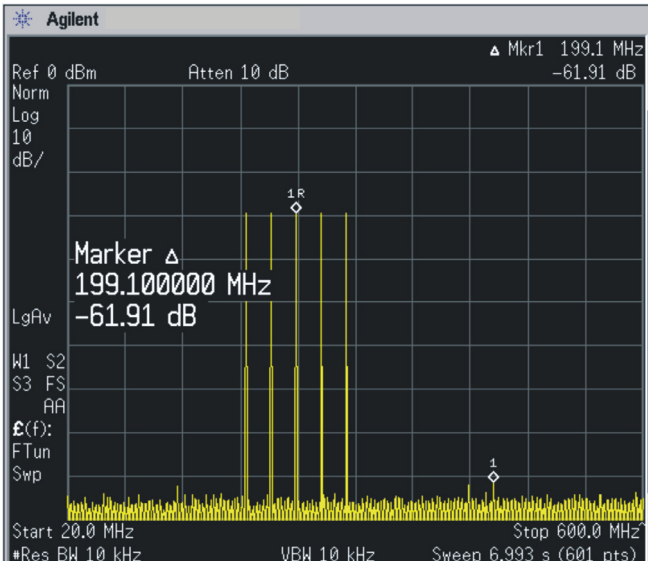
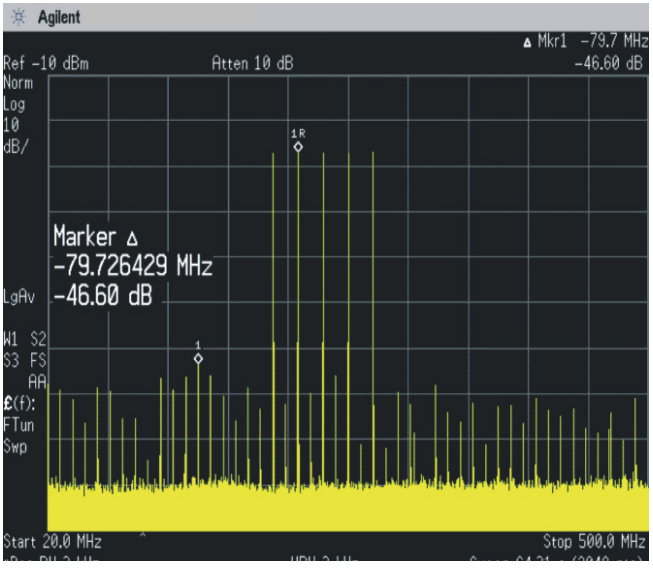
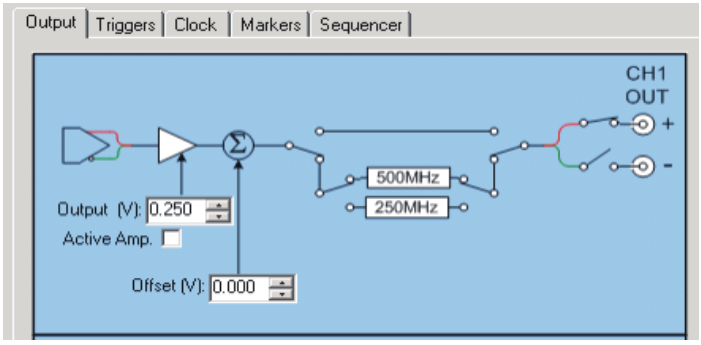



**Figure 2-4 N8241A Playback of Five Tones**



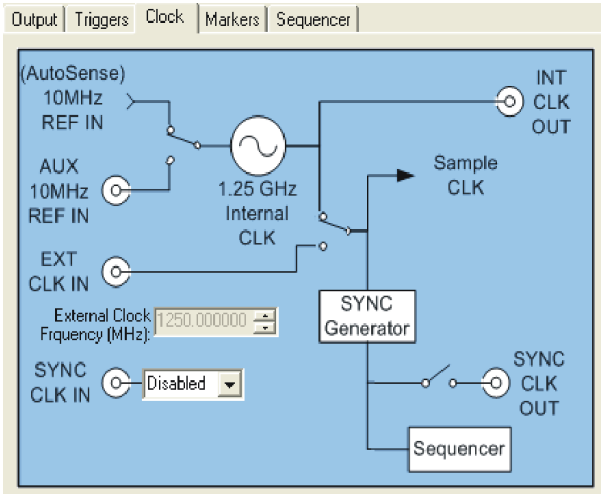
## Creating and Playing a Sequence

1. Connect the channel 1 positive (+) output to the spectrum analyzer RF input connector.
2. Open the user interface by double-clicking the **N8241A** icon placed on the desktop during installation.
3. Select the **Output** tab and connect a single-ended signal conditioning path to **CH1 OUT** (+) (click on the node that you want to connect).

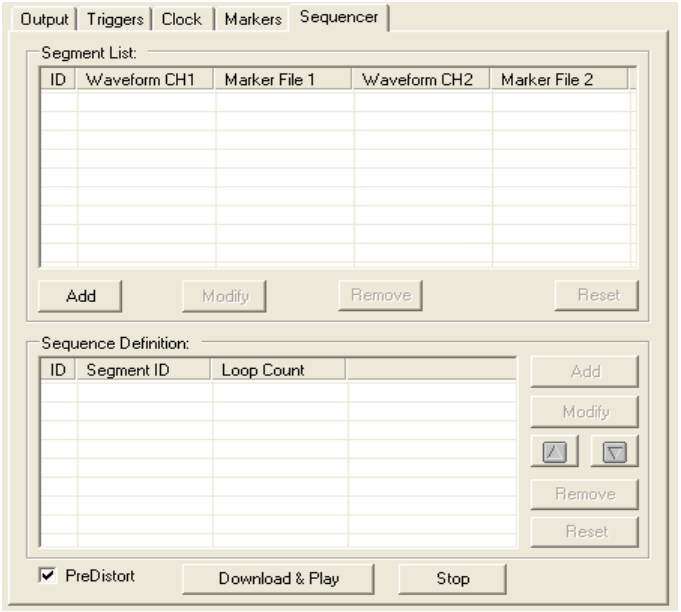



The connection will automatically enable differential mode. Click on the negative (-) node to enable single-ended mode.
.Notice that the default gain value was 0.500 volts. Once you select single-ended mode, the value drops to 0.250 volts. These are maximum values for the modes indicated.

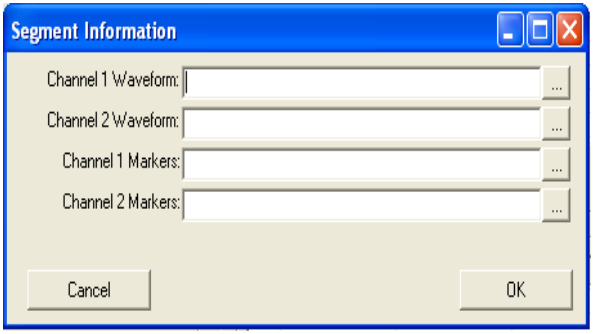
4. Select the **Clock** tab and confirm that the **(AutoSense) 10MHz REF IN** is configured correctly.



5. Select the **Sequencer** tab.




6. From the **Segment List** select **Add**. This will bring up a **Segment Information** secondary window.



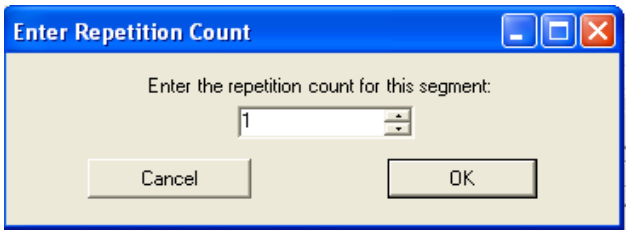

7. Browse and select the **500 MHz** waveform, then click **OK**.

**NOTE**

For dual channel sequencing, add the same waveform to both channel 1 and channel 2. Currently, the software does not support independent channel sequencing.

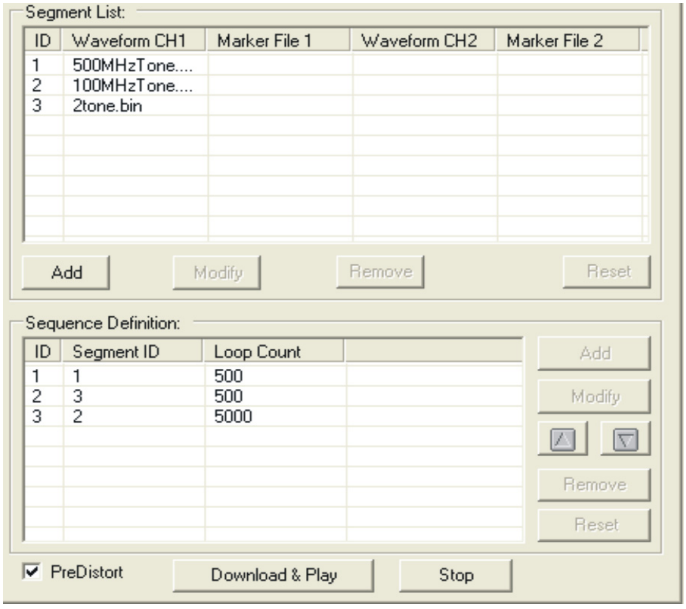
8. Repeat steps **6** and **7** twice, selecting the 100 MHz and two-tone waveforms.
9. In the **Segment List**, select the **500 MHz** waveform.
10. In the **Sequence Definition** area, select **Add**. This will bring up the

**Enter Repetition Count** secondary window.



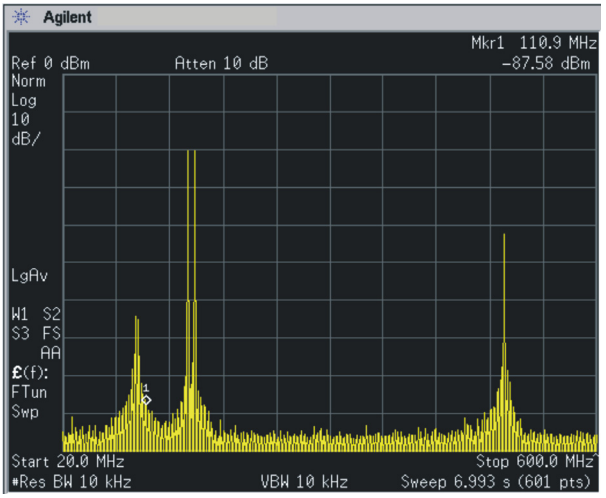

11. Enter **5000** repetitions and click **OK**.
12. Repeat steps **9**, **10**, and **11** for the 100 MHz and two-tone waveforms.
13. In the **Sequence Definition** area, select segment **ID 2** and move it below **ID 3** using the down arrow.
14. Click **Modify** and change the count to **50000**. The sequencer tab should look like Figure 2-5.

**Figure 2-5 Sequencer Tab**




15. Click **Download & Play**. The spectrum of the sequence should be similar to the one shown in Figure 2-6

**Figure 2-6** N8241A Playback of a Sequence



# Synchronizing Two N8241/2A Modules

## Internal Clock Synchronization Using Continuous Mode

When synchronizing two modules using the internal clock, one unit is designated as the Master and the other unit is designated as the Slave. The Master unit sources the sample clock and the sync clock signals. These signals are split and fed to the synchronized modules (the Master as well as the Slave).

The internal sample clock operates at 1.25 GHz and provides the final retiming of the analog output from each AWG. Any skew in the sample clock cable delays between the modules will result in the same skew in the analog outputs.The sample clock signal is split with a matched passive divider and the cable lengths are matched. The resulting skew is small and repeatable.

## Required Equipment

- Two N8241A or Two N8242A AWGs
- Personal Computer
- N8241A AWG Control Utility Software

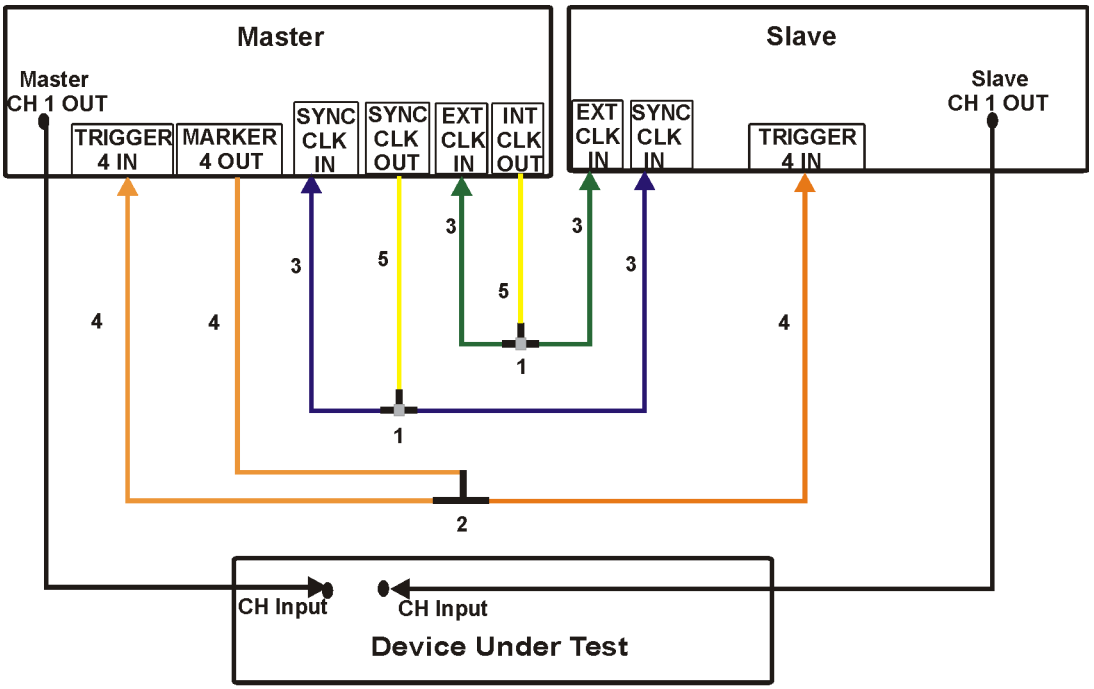
## Cables and Adapters required for 1.25 GHz external clock (Agilent N6030A K10 kit):

- Power divider, 11636B (2 each) (11636B)
- SMB adapter Tee M-M-M (1 each) (1250-0670)
- SMA conformable cable assembly, 10 in (4 each) (5062-6685)
- SMB cable assembly, (3 each) (8120-5016)
- SMA adapter M-F (2 each) (1250-1788)
- SMA to BNC Cable (2 each, equal length), Customer furnished

## Procedure Using a Software Marker

1. Start with the system turned off.
2. Cable the equipment as shown in Figure 2-7.

**Figure 2-7 Cabling for Two AWG Synchronization**




1 — Power divider
2 — SMB Adapter Tee
3 — SMA Cable Assembly 10 in
4 — SMB Cable Assembly
5 — Adapter

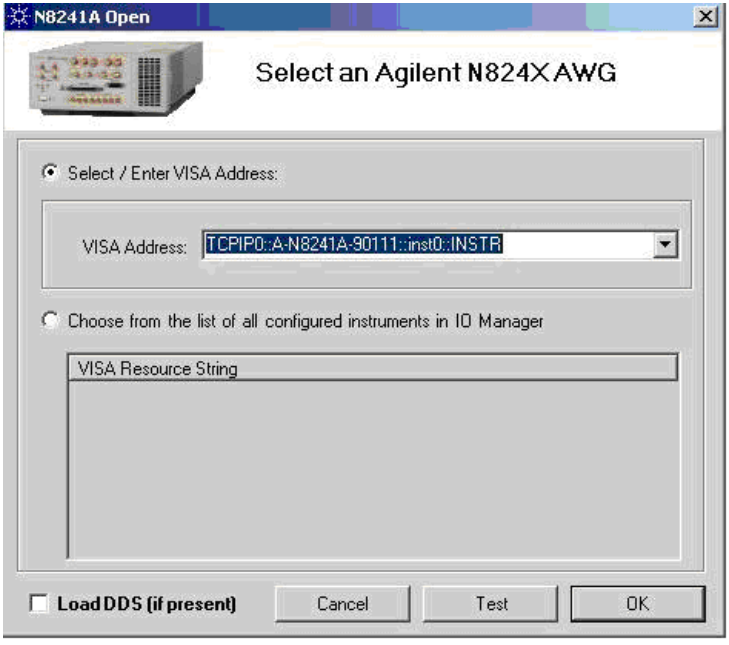
Note: The CH 1 OUT customer furnished cables from the Master and Slave modules must be of equal length.

3. Turn the system on.

### Selecting the Master Unit

1. Open an N8241A Control Utility session (double-click the Agilent N8241A icon on the desktop).
2. In the N8241A Open dialog, enter the VISA address for the master unit, then click **OK**.

**Figure 2-8 N8241A Selection Window**




3. Select the desired signal conditioning path
4. Select the desired waveform file.
5. Select the **Clock** tab.
6. From the **SYNC CLK IN** drop-down list, select **Master**.

Notice the following changes to the graphical user interface that are automatically configured when the Master unit is assigned:

### Clock Tab

- the internal clock is no longer driving the sample clock
- the sample clock and sync clock out are driven by the external clock in signal
- the sync clock in signal communicates with the sequencer

**Markers Tab**

- Marker 4 is assigned to a Software marker and is grayed out

**Triggers Tab**

- Start trigger is assigned to Trigger 4 and is grayed out

**Selecting the Slave Unit**

1. Open a second N8241A Control Utility session.
2. Highlight the unit designated as the **Slave** in the **N8241A Selection** window list and click **OK**.
3. Select the desired signal conditioning path.
4. Select the desired waveform file.
5. Select the **Clock** tab.
6. From the **SYNC CLK IN** drop-down list, select **Slave**.

Notice the following changes to the graphical user interface that are automatically configured when the Slave unit is assigned:

**Clock Tab**

- the internal clock is disabled
- the sample clock is driven by the external clock in signal
- the sync clock out is disabled
- the sync clock in signal communicates with the sequencer

**Triggers Tab**

- Start trigger is assigned to Trigger 4 and is grayed out

## Initiating Synchronous Playback

1. In the **Quick Play** area of the **Slave GUI**, select **Play**. This arms the waveform playback.
2. In the **Quick Play** area of the **Master GUI**, select **Play**. This initiates synchronous waveform playback.

**NOTE**

You can view the output on an oscilloscope by setting **Marker 1** on the **Master** module to **Waveform Start** and cabling the marker output to trigger the oscilloscope.

# Using Programmatic Interfaces

## IVI-C Driver Functionality

The IVI Foundation's class driver specification for function generators has been the model for the features in the N8241A and N8242A AWGs. This includes the recommended method to incorporate attributes for instrument-specific functions.

Please refer to *IVI-3.15 IviLxiSync Specification*, I*VI-4.3 IviFgen Class Specification*, and I*VI-3.1 Driver Architecture Specification* for more information. These can be found at:

www.ivifoundation.org/Downloads/Specifications.htm

A set of API Functions and Attributes can be found in the N8241A Help system. Go to:

**Start > Programs > Agilent > N8241A > Help**

or from the application menu bar

**Help > N8241A Online Help**

## MATLAB Interface

MATLAB is one of the programmatic interfaces supported by the N8241A and N8242A AWGs. Use the set of API functions to configure and play waveforms with the AWG. A complete list of the API functions can be found in the N8241A Control Utility in the Help menu. Go to:
**Help > N8241A Help > Programming > MATLAB API**.

To set up MATLAB for connectivity, while in the MATLAB environment, go to:

**File > Set Path > Add with Subfolders...**

navigate to your local drive and go to where your program files are stored. The default is:
**Program Files > Agilent > N8241A AWG > Matlab**
click **SAVE**, then **Close the Set Path** window.

MATLAB can now execute all of the N8241A API functions.

## MATLAB Example 1, Creating and Playing a Waveform

```
% N6030 Matlab Interface, Version 1.12
% Copyright (C) 2005, 2006 Agilent Technologies, Inc.
%
% A simple example of how to create a waveform, open a
% session to the Agilent N8241A AWG, play the waveform,
% and close the session.
% Note: the waveform must be configured before
downloading.
% If settings are changed after downloading the
waveform,
% the waveform must be re-downloaded.
%
% Create a waveform - a sine wave with 2000 pts
% Played at 1250 MHz, this will produce a tone of 1.250
MHz


numberOfSamples = 2000;
samples = 1:numberOfSamples;
ch1 = sin(2 * samples/numberOfSamples * 2*pi);
ch2 = cos(2 * samples/numberOfSamples * 2*pi);
waveform = [ch1; ch2];


% Open a session
disp('Opening a session to the instrument');
[instrumentHandle, errorN, errorMsg] =
agt_awg_open('TCPIP','TCPIP0::A-N8241-90XXX::inst0::INST
R');
if(errorN ~= 0)
   % An error occurred while trying to open the session.
    disp('Could not open a session to the instrument');
    return;
end
```

```
disp('Enabling the instrument output');
[errorN, errorMsg] = agt_awg_setstate(instrumentHandle,
'outputenabled', 'true');
if(errorN ~= 0)
   % An error occurred while trying to enable the output.
    disp('Could not enable the instrument output');
    return;
end

disp('Setting the instrument to ARB mode');
[errorN, errorMsg] = agt_awg_setstate(instrumentHandle,
'outputmode', 'arb');
if(errorN ~= 0)
    % An error occurred while trying to set the ARB mode.
    disp('Could not set the instrument to ARB mode');
    return;
end

disp('Transfering the waveform to the instrument');
[waveformHandle, errorN, errorMsg] =
agt_awg_storewaveform(instrumentHandle, waveform);
if(errorN ~= 0)
    % An error occurred while trying to transfer the
waveform.
    disp('Could not transfer the waveform to the
instrument');
    return;
end

disp('Initiating playback of the waveform on the
instrument');
```

```
[errorN, errorMsg] =
agt_awg_playwaveform(instrumentHandle, waveformHandle);

if(errorN ~= 0)

    % An error occurred while trying to playback the
waveform.

    disp('Could not initiate playback of the waveform on
the instrument');

    return;

end


disp('Press ENTER to close the instrument session and
conclude this example.');

pause;


agt_awg_close(instrumentHandle);

disp('Session to the instrument closed successfully.');
```

## MATLAB Example 2, Synchronizing Two N8241/2A AWGs

```
MATLAB Example 2, Synchronizing Two AWG Modules

% N6030 Matlab Interface, Version 1.12
% Copyright (C) 2005, 2006 Agilent Technologies, Inc.
%
% This example initiates dual module synchronized
waveform
% playback.
%
% Use agt_awg_browse to identify the modules.
%
% Create a waveform - a sine wave with 2000 pts
% Played at 1250 MHz, this will produce a tone of 1.250
MHz
numberOfSamples = 2000;
samples = 1:numberOfSamples;
ch1 = sin(2 * samples/numberOfSamples * 2*pi);
ch2 = cos(2 * samples/numberOfSamples * 2*pi);
waveform = [ch1; ch2];
```

```
% Try to open a session
disp('Opening a session to the instrument');
    [instrumentHandle2, errorN, errorMsg] =
agt_awg_open('TCPIP','TCPIP0::A-N8241-90XXX::inst0::INST
R');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end


    [instrumentHandle1, errorN, errorMsg] = agt_awg_open
('TCPIP','TCPIP0::A-N8241-90XXX::inst0::INSTR');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end


disp('Enabling the instrument output');
    [errorN, errorMsg] =
agt_awg_setstate(instrumentHandle1, 'outputenabled',
'true');
        if errorN ~= 0
            disp(errorN);
```

```
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end


    [errorN, errorMsg] =
agt_awg_setstate(instrumentHandle2, 'outputenabled',
'true');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end


disp('Setting the instrument to ARB mode');
    [errorN, errorMsg] =
agt_awg_setstate(instrumentHandle1, 'outputmode',
'arb');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end
```

```
    [errorN, errorMsg] =
agt_awg_setstate(instrumentHandle2, 'outputmode',
'arb');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


disp('Setup the Master');
    [errorN, errorMsg] =
agt_awg_setstate(instrumentHandle1, 'syncmode',
'master');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


disp('Setup the Slave');
    [errorN, errorMsg] =
agt_awg_setstate(instrumentHandle2, 'syncmode',
'slave');
        if errorN ~= 0
            disp(errorN);
```

```
            disp(errorMsg);
            disp('proram stopped');
            return
        else
            disp('ok');
        end


disp('Transfering the waveform to the instrument');
    [waveformHandle, errorN, errorMsg] =
agt_awg_storewaveform(instrumentHandle1, waveform);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


    [waveformHandle, errorN, errorMsg] =
agt_awg_storewaveform(instrumentHandle2, waveform);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


disp('Initiating playback of the waveform on the
```

```
instrument');
    [errorN, errorMsg] =
agt_awg_playwaveform(instrumentHandle2, waveformHandle);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end

    [errorN, errorMsg] =
agt_awg_playwaveform(instrumentHandle1, waveformHandle);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end

disp('Init Generation');
    [errorN, errorMsg] =
agt_awg_initiategeneration(instrumentHandle2);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
```

```
        else
            disp('ok');
        end


    [errorN, errorMsg] =
agt_awg_initiategeneration(instrumentHandle1);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


disp('Press ENTER to close the instrument session and
conclude this example.');
```

## C/C++ Example Program

```
/* Example for programming the N8241A IVI-C driver.
Copyright (C) 2005, 2006 Agilent Technologies, Inc.

This will compile and link into a working.EXE file.

For Compile: Add include path = C:\Program
Files\IVI\include,

C:\vxipnp\winnt\include

For Link: Add libpath = C:\Program Files\IVI\Lib\msc,
Add lib = AGN6030A.lib

Opening a session with predistortion enabled (default)
creates a discrepancy for the waveform in ch2 since
predistortion is applied twice; once when it was
downloaded to ch1 and again when it is downloaded to ch2.

You can eliminate this problem by turning off the
predistortion before downloading the waveform to ch2. An
alternative is to clone the waveform to another file
name. For example, clone Wfm_ch1 to Wfm_ch2.

*/

#include <math.h>

#include <windows.h>

#include <winbase.h>

#include <AGN6030A.h>

// #include "stdafx.h" // if you use Microsoft
// Visual Studio you might use this

#define WFM_LENGTH 800 //should be integer divisible by
16

int main(int argc, char* argv[])

{

ViStatus rc;

ViRsrc resourceName =
"TCPIP0::A-N8241-90XXX::inst0::INSTR"; // Set
// this to match your hardware

ViBoolean IDQuery = VI_FALSE;
```

```
ViBoolean resetDevice = VI_TRUE;
ViSession session = 0;
ViInt32 wfmHandle1;
ViInt32 wfmHandle2;
int i;
double twopi;
double ifWfm[WFM_LENGTH];
double Fsig = 500e6; // Set this to a CW frequency
// <= 500 MHz
double Fs = 1.25e9; // Sample Clock Frequency
// Initialize N8241A and setup session handle
rc = AGN6030A_init(resourceName, IDQuery, resetDevice,
&session);
if (rc != VI_SUCCESS)
return -1;
// Setup some Channel 1 states
// Set to single-ended operation, filter on,
// 500 MHz filter selected
rc = AGN6030A_ConfigureOutputConfiguration(session, "1",
AGN6030A_VAL_CONFIGURATION_SINGLE_ENDED,
VI_TRUE, 500e6);
if (rc != VI_SUCCESS)
return -1;
// Set output to ON
rc = AGN6030A_ConfigureOutputEnabled(session, "1",
VI_TRUE);
if (rc != VI_SUCCESS)
return -1;
// Do the same for Channel 2
rc = AGN6030A_ConfigureOutputConfiguration(session, "2",
AGN6030A_VAL_CONFIGURATION_SINGLE_ENDED,
VI_TRUE, 500e6);
```

```
if (rc != VI_SUCCESS)

return -1;

rc = AGN6030A_ConfigureOutputEnabled(session, "2",
VI_TRUE);

if (rc != VI_SUCCESS)

return -1;

// Select the Internal Sample Clock and an
//External Reference Clock

rc = AGN6030A_ConfigureSampleClock(session,
AGN6030A_VAL_CLOCK_INTERNAL, Fs);

if (rc != VI_SUCCESS)

return -1;

// This uses the front panel 10MHz REF IN

// connection. To use the PCI backplane clock,
// substitute AGN6030A_VAL_REF_CLOCK_PXI

rc = AGN6030A_ConfigureRefClockSource(session,
AGN6030A_VAL_REF_CLOCK_EXTERNAL);

if (rc != VI_SUCCESS)

return -1;

// Enable or disable built-in corrections.
// Default is enabled. This attribute is not
// available in release 1.00.

/* rc = AGN6030A_SetAttributeViBoolean(session, NULL,
AGN6030A_ATTR_PREDISTORTION_ENABLED,

VI_TRUE);

if (rc != VI_SUCCESS)

return -1;

*/

// Build a sample waveform for testing.
// This produces a CW tone at Fsig Hz.

twopi = 8.0 * atan(1.0);

for (i = 0; i < WFM_LENGTH; i++)

{
```

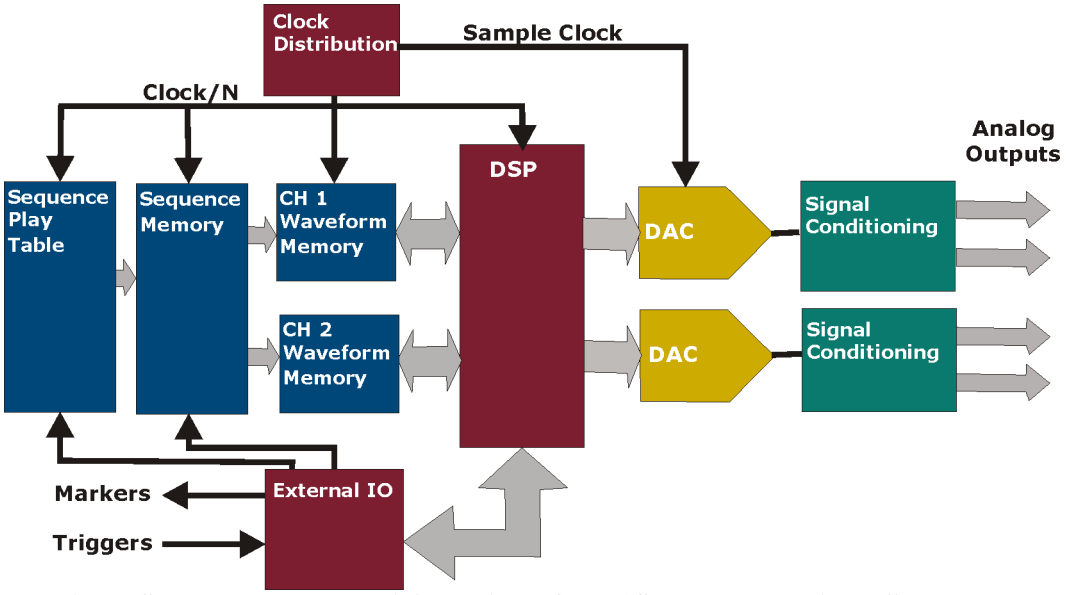
```
ifWfm[i] = sin(twopi * (Fsig/Fs) * (double)i);
}
// Set N8241A output mode to ARB in preparation of
// downloading and playing our waveform.
rc = AGN6030A_ConfigureOutputMode(session,
AGN6030A_VAL_OUTPUT_ARB);
if (rc != VI_SUCCESS)
return -1;
// Download the waveform to both channels 1 and 2
// even if 2is not used. This is a requirement at
// this time and must be followed!! To do this,
// call the function twice and discard the second
// waveform handle if Channel 2 is not used.
rc = AGN6030A_CreateArbWaveform(session, WFM_LENGTH,
ifWfm, &wfmHandle1);
if (rc != VI_SUCCESS)
return -1;
rc = AGN6030A_CreateArbWaveform(session, WFM_LENGTH,
ifWfm, &wfmHandle2);
if (rc != VI_SUCCESS)
return -1;
// Configure N8241A to play downloaded waveforms.
// Set to 250 mV gain and 0V offset.
rc = AGN6030A_ConfigureArbWaveform(session, "1",
wfmHandle1, 0.250, 0.0);
if (rc != VI_SUCCESS)
return -1;
rc = AGN6030A_ConfigureArbWaveform(session, "2",
wfmHandle2, 0.250, 0.0);
if (rc != VI_SUCCESS)
return -1;
// Close the open session
rc = AGN6030A_close(session);
return 0;
```

```
}
```

# 3 Theory of Operation

This chapter includes the following topics that explain the theory behind the functionality of the N8241A and N8242A Arbitrary Waveform Generators.

# N8241/2A Block Diagram




**N is the Sync clock prescaler divide ratio. Refer to "Synchronous Triggers".**

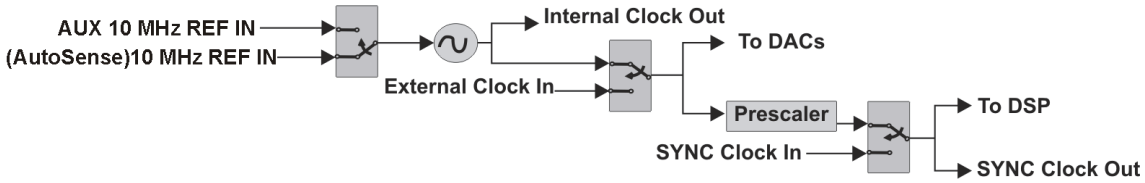
The N8241A and N8242A Arbitrary Waveform Generators (AWGs) are dual channel AWGs that offer wide bandwidth as well as excellent signal fidelity. The AWG was developed incorporating a high performance Agilent digital-to-analog converter (DAC) designed to clock up to 1.25 GHz. The N8241A has 15 bits of vertical resolution and the N8242A 10 bits. The DACs are fully differential and the AWGs support both single-ended and differential outputs through the analog signal conditioning path.

The AWGs support advanced sequencing and triggering modes that enable event-based signal simulations. The DSP forms the heart of the sequencer storing the information used to define the order that stored waveforms are played.

The AWGs are also designed to enable synchronization of multiple units.

# Clock I/O

## 10 MHz In




A 10 MHz reference is required when using the internal clock. You can use either the (AutoSense) 10 MHz REF IN (the default) or the AUX 10 MHz REF IN connector to supply the 10 MHz reference.

The high-performance 1.25 GHz oscillator provides the internal sample clock for the module.

## Internal Clock Out

The 1.25 GS/s low noise internal sample clock is output through the INT CLK OUT connector and can be routed to other AWGs or test equipment. The internal clock output is available even when an external clock is used.

## External Clock

An external sample clock can be input through the EXT CLK IN connector. The external sample rate must be within the range of 100 MS/s and 1.25 GS/s. To achieve the optimal signal performance on the AWG analog output, use an external clock with a phase noise floor below -155 dBc/Hz and a power setting of approximately 0 dBm.

**NOTE** An error message will appear if the clock rate does not match the hardware setting, or an external clock is not present.

## SYNC Clock In/SYNC Clock Out

The SYNC CLOCK IN and SYNC CLOCK OUT are used for the synchronization of multiple modules. Refer to "Synchronization Using an Internal Clock" on page 87 and "Synchronization Using an External Clock" on page 88.

# Waveform Playback

## Waveforms

Single waveforms are played back in one of two modes:

- **Continuous**
  The waveform repeats indefinitely.
- **Burst**
  Once a trigger is received, the waveform repeats a specified number of times.

## Waveform Sequencer Function

Sequencing provides a method of waveform memory compression using a play table, sequencer memory, and waveform memory. The sequencer controls how waveforms are accessed and performs the following functions:

- determines the order of play for waveforms stored in memory
- enables the construction of long waveforms from shorter or repeated segments
- responds to external triggers
- offers several modes of segment advance
- outputs markers

## Sequence Play Table

The play table contains entries that point to sequences in the sequencer memory. Within the play table you can have up to 16384 sequence pointers.

## Sequencer Memory

The sequencer memory contains instructions on how to play through the waveform memory. It can hold up to 32768 segments (waveforms with a specified loop count).

## Waveform Memory

The waveform memory contains Channel 1 and Channel 2, and output marker data.

**NOTE** The N8241A Control Utility GUI only supports basic sequencing. Advanced sequencing features can only be accessed through the programmatic interfaces.

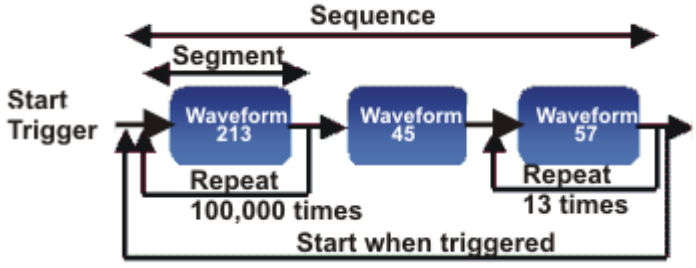
## Basic Sequencing

A sequence is a sequential list of segments and may occur anywhere in the sequence memory. A sequence may have a preamble of one or more segments that is played once at the start of the sequence, but not repeated until the sequence is started again.

Waveforms are stored in dedicated banks of memory for channel 1 and channel 2. The waveform playback of each channel is directly controlled by the sequencer. The sequencer supplies the memory pointers necessary to create analog signals from the digital data stored in memory. In addition, the sequencer provides the capability to create sequences made of multiple waveform segments. This is helpful when constructing long waveforms with repeating segments. A long waveform might consist of repetitive data that can be stored as single segments and repeated in the sequencer. This extends the waveform play time achievable with the available memory.

Basic sequencing can be done using the software N8241A Control Utility GUI or through the programmatic interfaces.

**Figure 3-1** **Example Sequence**




### Playback

There are two playback modes for basic sequencing:

- **Continuous**
  The sequence repeats indefinitely or until an event trigger is received.
- **Burst**
  The sequence is repeated a predefined number of times. This mode requires a start trigger.

A total of 16,000 unique waveform sequences can be defined. Segments have a minimum length of 128 samples and a granularity of 8 samples. A sequence must contain at least two segments and can have up to the maximum number of 32768

segments. Each waveform segment is played out according to its segment and sequence definition. A total of 1 million (220) loops can be defined for each segment. After the last segment loop is executed, the entire sequence can repeat continuously or for the predefined number of times.

## Advanced Sequencing

**NOTE** Advanced sequencing is only available through the programatic interfaces.

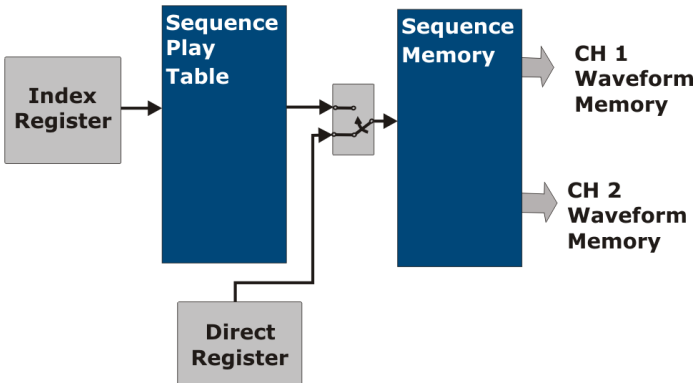
Advanced sequencing enables the grouping of sequences into scenarios in a way that is similar to how segments are grouped in sequencing. With scenarios you gain more control of waveform playback.

### Scenario Pointer Source

There are two ways to choose which sequence to play.

- **Index**
  A register is written to by the host processor that addresses entries in the sequence play table. This register can be written to at any time including while a sequence is playing. A valid Start trigger or Jump trigger starts the sequence specified by the index in the register. The valid sequence index range is 0-16383. Selecting invalid sequence indexes causes indeterminate behavior.

- **Direct**
  The user can directly address waveforms in the sequencer memory completely bypassing the play table. The next sequence pointer can be written to while a sequence is being played. A valid Start trigger or Jump trigger starts the sequence specified by the new pointer in the register. Addressing undefined sequences causes indeterminate behavior.



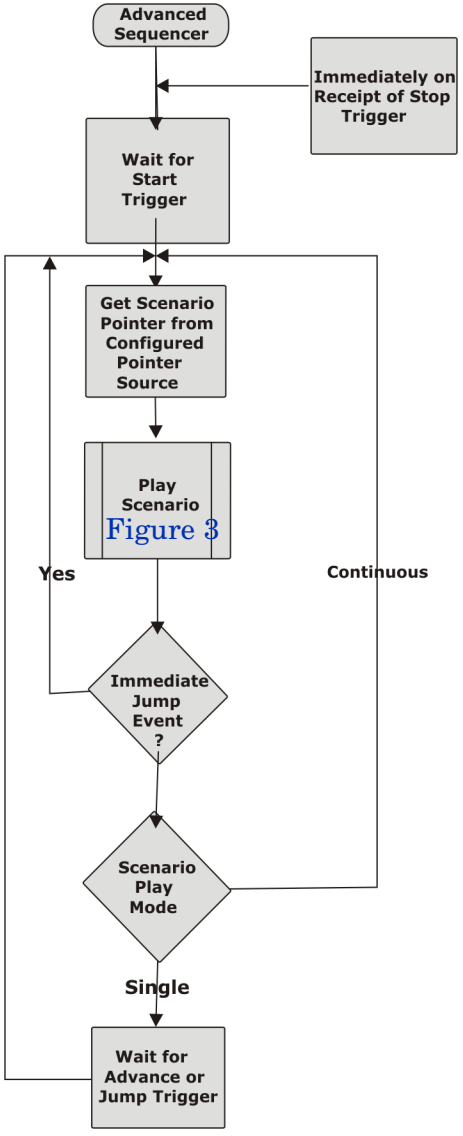
### Scenario Advance Mode

The play table can be configured to play a scenario once or continuously after starting.

- **Single**
  The scenario plays once and then waits for a trigger. While waiting for a trigger, the value of the last waveform continues to play. If the scenario pointer does not change, a Start trigger or Jump trigger causes the scenario to play again. If the scenario pointer changes, the next Start trigger or Jump trigger will start the new scenario. The effect of a scenario jump trigger received before the end of the scenario is determined by the scenario jump mode.
- **Continuous**
  The scenario repeats indefinitely until it is stopped or a scenario jump trigger is received.
  The scenario exit is dependent on the scenario jump mode.

  Refer to "Advanced Sequencer Flow Chart" on page 74.

**Figure 3-2** **Advanced Sequencer Flow Chart**



### Waveform Advancement

In basic sequencing, waveforms always advance to the next waveform automatically after the specified number of repetitions. With advanced sequencing, waveforms can be configured to advance in one of four ways:

- **Automatic**
  The waveform automatically advances to the next waveform after completing the specified number of loop repetitions.
- **Continuous**
  The waveform loop is repeated continuously until a trigger is received. The current loop is finished before advancing to the next waveform. The waveform loop repetition count is ignored.
- **Single**
  The waveform loop plays once and waits at the end of the loop for a trigger. The waveform loop is repeated for each trigger until the number of waveform loop repetitions is met. The next trigger will advance to the next waveform. When the waveform loop repetition count is one, a single trigger will advance to the next waveform. While waiting for a trigger, the last value of the waveform loop continues to play.
- **Repeat**
  The waveform loop repeats until the number of waveform loop repetitions is met.

### Scenario Jump Mode

The scenario jump mode determines how the play table responds to a scenario jump input. There are no discontinuities in a scenario jump, other than those imposed by the waveform data. A scenario jump has very predictable behavior. For scenario jumping to be valid, the scenario length must be equal to or greater than the jump immediate latency.

There are three types of jump modes:

- **Immediate**
  The scenario starts or jumps immediately with latency.
- **End of Waveform**
  The current waveform, including repeats, is completed before jumping to the new scenario.The jump latency is the longer of either the jump immediate latency or the length of the remaining part of the current waveform. If the remaining part of the scenario is less than the jump immediate latency, the scenario is repeated one more time before jumping.

- **End of Scenario**
  The current scenario is completed before jumping to the new scenario. The jump latency is the longer of either the jump immediate latency or the length of the remaining part of the current waveform. If the remaining part of the scenario is less than the jump immediate latency, the scenario is repeated one more time before jumping.

### Scenario Start/Jump Trigger Source

It is possible to start a scenario, or to jump to a new scenario using one of five inputs. There are four external trigger inputs and a host trigger source. The host trigger source is a register in the play table that can be written to by the host processor. The host processor provides the user a way to start the scenario, or create a jump event. The latency for a scenario jump is established by the jump mode.

Refer to "Waveform Play Flow Chart" on page 77 and "Scenario and Sequence Play Flow Charts" on page 78.

The Jump Trigger condition is satisfied either by a waveform jump event, or by a scenario jump trigger event when the scenario jump mode is set to "End of Waveform."

**Figure 3-3** Waveform Play Flow Chart

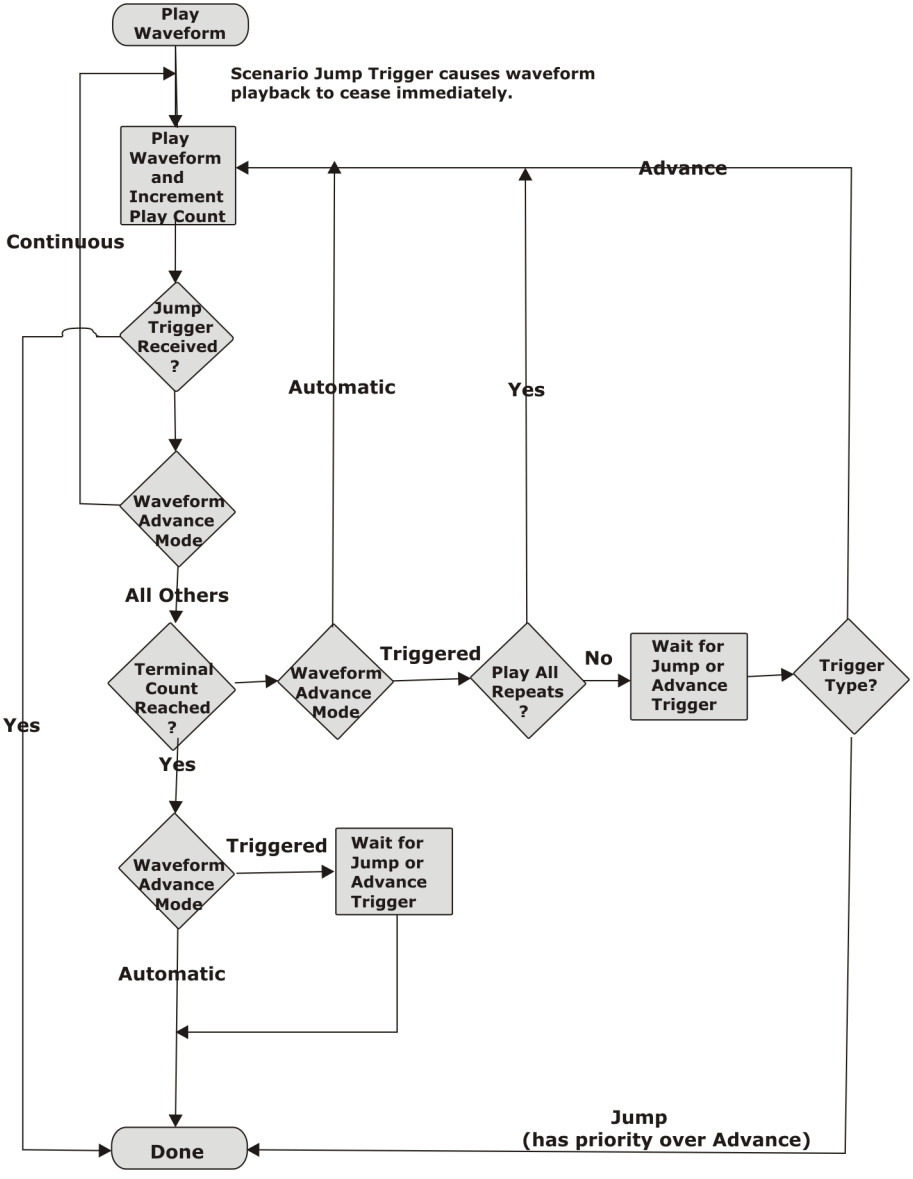
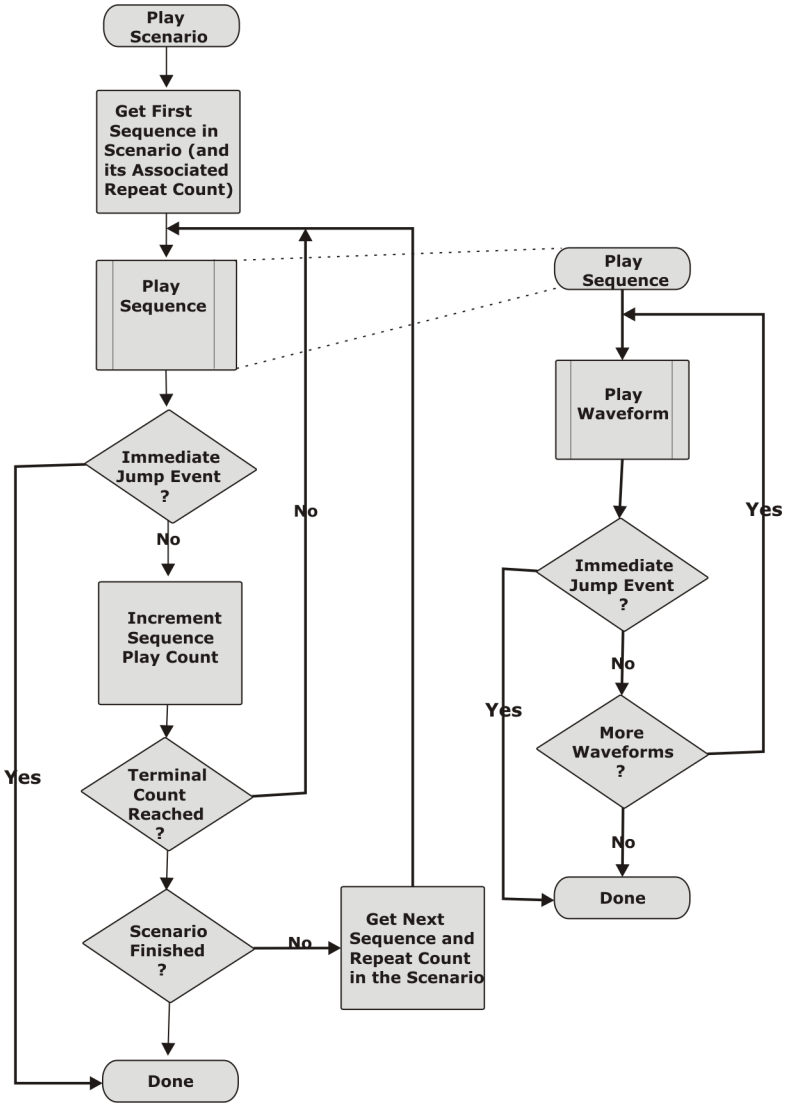


**Figure 3-4** **Scenario and Sequence Play Flow Charts**



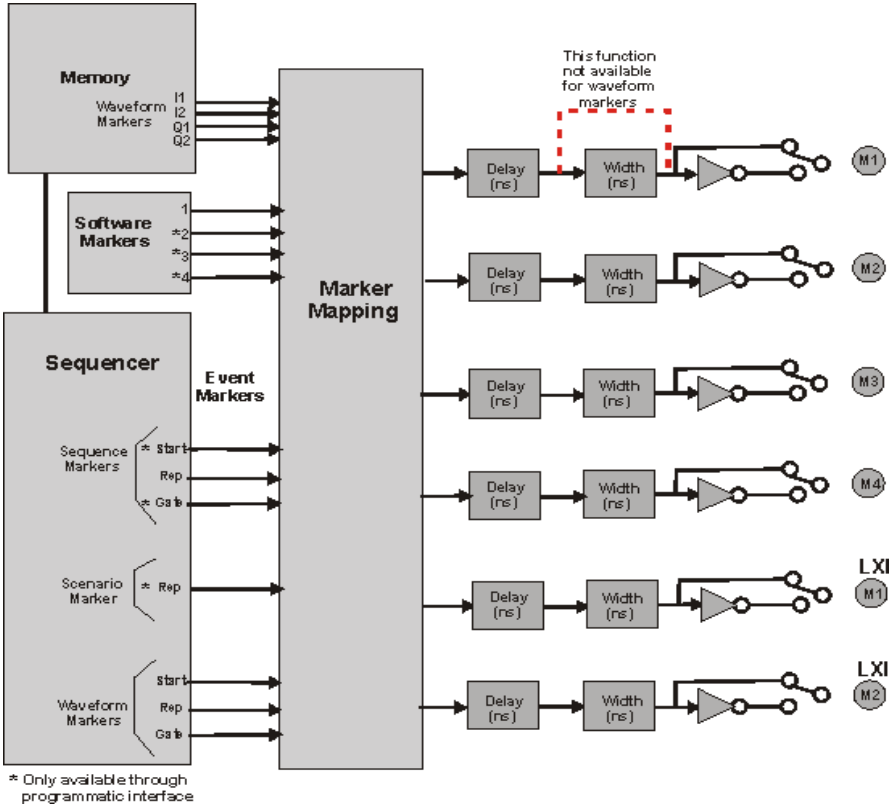
## Markers

The N8241/2A AWG provides four front panel marker output connectors that can be used for system synchronization and triggering. The following markers can be enabled:

- Ch 1 Memory Marker 1 and Memory Marker 2
- Ch 2 Memory Marker 1 and Memory Marker 2
- Waveform Start, Repeat, and Gate
- Sequence Start, Repeat, and Gate
- Scenario Repeat
- Software

Marker outputs are aligned with the analog output of the AWG.

**Figure 3-5** **Marker Block Diagram**




In addition, two LXI markers are available for routing to the LXI Trigger Bus or the

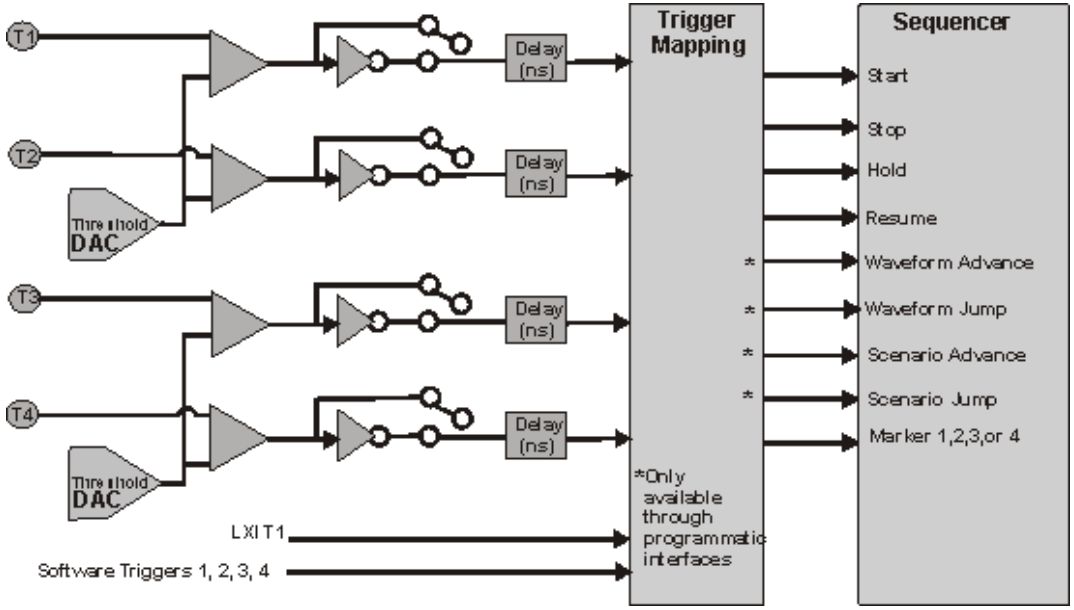
front panel trigger out connector. There are 16 marker output selections for the LXI trigger bus; LAN 0–7 and LXI 0–7.

Markers can be set in the sequencer to be at any point in the data with a positive or negative polarity. Marker widths, except those derived from waveform memory, can be set in increments of the SYNC clock (-8 to 247 clocks). The marker delay function uses the input value to calculate the delay to the nearest 1/4 SYNC clock cycle. The sequencer is capable of outputting nine markers, which can be multiplexed to the four marker outputs. The Sequence Start, Sequence Gate, Scenario Repeat, and three software markers are only available through the programmatic interfaces.

## Triggers

The AWG module has five front panel trigger input connector, a rear panel LXI trigger bus, and triggering through the LAN line. All triggers passing through the LXI trigger bus and the LAN line are executed through the LXI T1 trigger.

**Figure 3-6** **Trigger Block Diagram**



### Triggers 1,2,3,4

These four trigger inputs can be used to control waveforms in the sequencer. Hardware trigger inputs may be configured to generate events on the rising or falling SYNC clock edges, but not both at the same time. The trigger threshold can be set between –4.5 and +4.5V. Ports 1 and 2 have a common threshold, and ports 3 an 4 have a common threshold. These two common thresholds are not shared and can be set independently.

Trigger delays can be set in increments of the SYNC clock (0-255 clocks).

These trigger inputs can be configured to initiate the following events through the software Control Utility:

| | |
|---|---|
| Start | starts playback at the beginning of the waveform |
| Hold | holds at the end of the waveform |
| Stop | stops playback |
| Resume | resumes playback at the point in the waveform that play was held or stopped |

The Waveform Advance, Scenario Advance, Waveform Jump, and Scenario Jump triggers are only available through the programatic interfaces.

### LXI T1

These trigger inputs can be configured to the following:

| | |
|---|---|
| LAN 0-7 | provides a way to trigger programmatically over a LAN line |
| LXI 0-7 | the LXI Trigger Bus enables event driven functionality over an eight channel multipoint LVDS system that can simultaneously transmit and receive signals |
| Trigger In | direct trigger |

**NOTE** To achieve the specified performance, use front panel triggers 1, 2, 3, or 4. Triggers over the Trigger In and LXI Trigger Bus will have more latency than what is specified for Triggers 1-4. Triggers over the LAN will experience the most latency.

## Synchronous Triggers

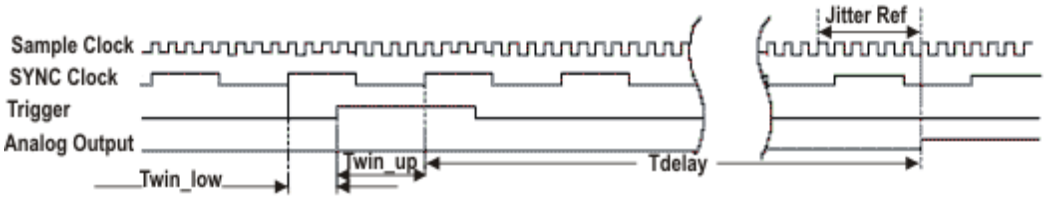
Triggers are registered into the AWG using the SYNC clock. The SYNC clock is nominally at the sample clock frequency divided by 8. However, at lower sample rates an internal variable modulus prescaler selects other binary divide ratios: 4, 2, and 1. In general, the SYNC clock frequency is always in the range of 78.13 MHz to 156.25 MHz. The input clock frequency ranges and prescaler divide ratios are as specified in Table 3-1:

**Table 3-1 Synchronous Triggers**

| Sample Clock Frequency | SYNC Clock Prescaler Divide Ratio |
|---|---|
| 625 MHz - 1.25 GHz | 8 |
| 312.5 MHz – 625 MHz | 4 |
| 156.25 MHz – 312.5MHz | 2 |
| 100 MHz – 156.25 MHz | 1 |

It is necessary to insure that the correct timing relationships are achieved to guarantee consistent synchronous trigger operation. The trigger input must occur within a valid window with respect to the SYNC clock. The window is specified by two times: Twin_low —the minimum trigger delay after the prior SYNC clock edge; and Twin_up — the minimum trigger setup before the next SYNC clock edge. These are specified for the trigger input relative to the SYNC clock output. The trigger must be a minimum of two SYNC clock cycles long. The trigger timing is specified relative to the rising edge of the SYNC clock. The analog output from the AWG is then produced a fixed number of sample clock cycles (plus a small fixed propagation delay) after the first rising edge of the SYNC clock after the trigger goes active. Since the analog output is retimed by the sample clock, the reference for jitter measurements is the sample clock, as shown in the Figure 3-7. You can use an input trigger to generate an output marker to synchronize triggers since marker outputs are aligned with the analog output of the AWG.

**Figure 3-7** **Synchronous Trigger Timing Diagram**

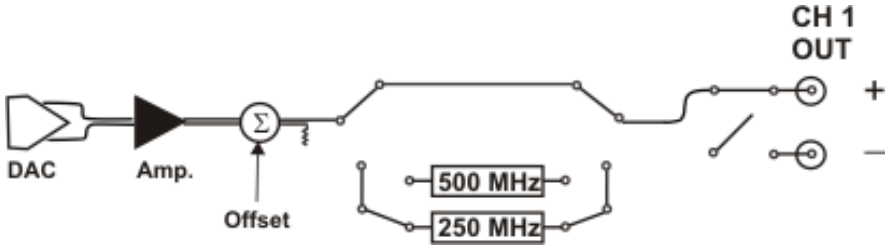


# Signal Conditioning

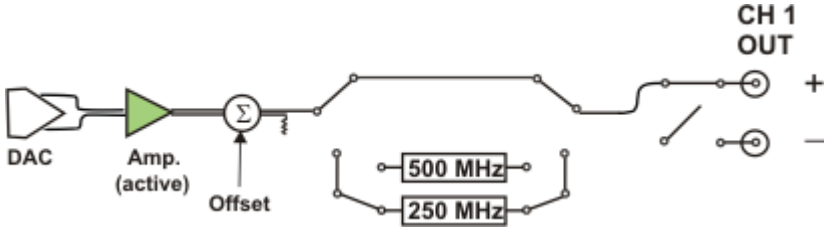
## Single-Ended Mode

Single-ended mode has two modes of operation with signal output through the positive (+) port. The negative port (-) is reserved for differential mode.

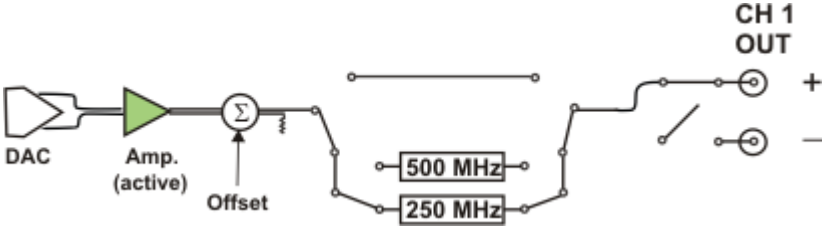
Passive mode has an adjustable output level of up to 0.5Vp-p
This mode gives the greatest single-ended signal fidelity because there is a balun in the path that suppresses the second order harmonic.




Active mode has an output level of up to 1.0Vp-p and ±0.2Vp-p offset range when the amplifier is activated. The active mode trades off signal fidelity for an increase in signal power.



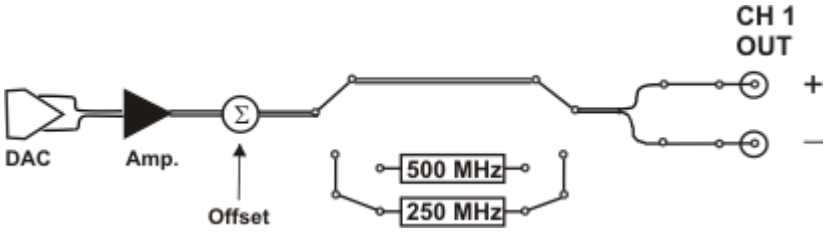

There are two internal reconstruction filters, 250 MHz and 500 MHz, that can be inserted in the signal path of either mode.



## Differential Mode

The differential mode has an output level of up to 0.5Vp-p. This mode provides exceptional signal fidelity into true differential inputs (which provide common mode rejection). A larger differential output voltage is also obtained without the use of the amplifier. To preserve signal purity, the active amplifier cannot be used in differential mode. Differential mode is not recommended when driving single-ended loads since the second order distortion is degraded. If you choose to drive single-ended loads, you must terminate the negative (-) port of the channel with a 50 ohm load.

Adjustable output voltage and offsets as well as reconstruction filters can be used in differential mode



# Digital Predistortion

The predistortion function compensates for the variation in the magnitude of the output response as a function of frequency. This variation is the result of the sin x/x (sinc) roll-off of the internal DAC and the frequency response of the reconstruction filter. The correction method uses filters to level the amplitude response and to create a linear phase response at the front panel of the AWG. This process attenuates the signal as a function of frequency, but cannot increase the signal above the maximum output voltage. Therefore, it is necessary to attenuate the lower frequency signals. This results in a reduced output voltage and dynamic range at all frequencies, but with uniform response across the full frequency range.

# Multiple Module Synchronization

Within each AWG, the two channels are synchronized by design. Some systems, such as phased array radar, require more than two synchronized channels. The AWG is designed to support the synchronization of up to 16 channels through the use of eight AWGs. Synchronization of multiple AWGs can be achieved using either the internal clock or an external clock.

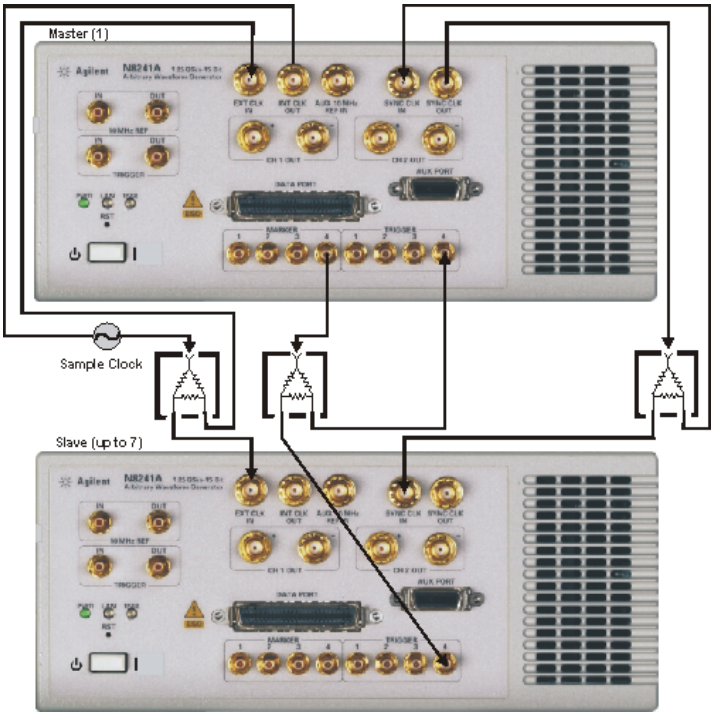
## Synchronization Using an Internal Clock

In synchronizing multiple modules using the internal clock, one unit is designated as the Master and the other units are designated as Slave units. The Master unit sources the following signals: Sample clock, SYNC clock, and the Sync Marker. These signals are all split and fed to each of the synchronized modules (the Master as well as the Slaves).The internal sample clock is at 1.25 GHz. The sample clock provides the final retiming of the analog output from each AWG. Any skew in the sample clock cable delays between the multiple modules will result in the same skew in the analog outputs.

Typically, the sample clock signal is split with a matched passive splitter and the cable lengths are matched to better than 5 mm. The resulting skew is small and repeatable. If desired, the skew can be measured and calibrated (along with any phase shifts in cables on the AWG outputs) by adding fixed delay offsets to the waveforms.

The SYNC clock is used internal to the AWG to clock the internal data generator and to clock in the synchronous triggers. When using the internal clock, the SYNC clock has a frequency of 1/8th the sample clock rate (156.25 MHz). When synchronizing multiple units, the SYNC clock output must be enabled in software (in the Master) and the external SYNC clock input selected in all the modules. The SYNC clock signal is split passively and distributed with low skew. The SYNC clock output level and the input sensitivity support up to a 1 to 8 split (fan-out) using matched 50 Ohm splitters (6 dB loss per 1 to 2 splitter). There is a specific SYNC cable length that is required as a function of the sample clock frequency. Several different lengths can be used, provided they are integer multiples of one half of a SYNC clock period.

**Figure 3-8** **Cabling for Internal Clock Synchronization**




The trigger cables should all be the same length. The trigger inputs are high impedance and several inputs can be driven in parallel without matched passive splitters. The synchronous trigger timing can be determined in the same way as any synchronous trigger into the AWG. The timing is specified relative to the SYNC clock out. This is easily observed on the slave modules, where the SYNC clock out is unconnected.

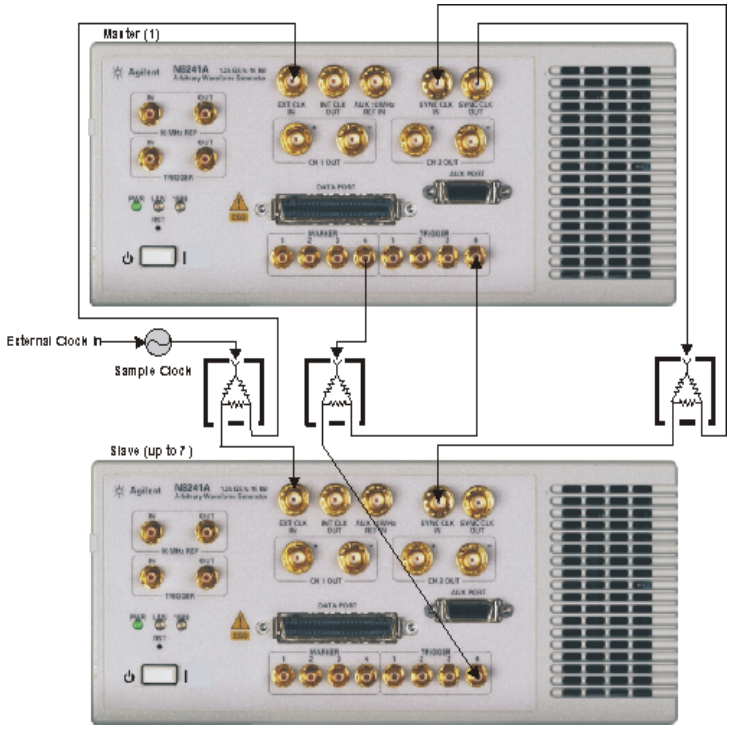
The multiple AWGs are configured to have an internal start trigger to begin play. A software start marker event is used to initiate the synchronized play. Marker 4 and Trigger 4 are used for this purpose.

## Synchronization Using an External Clock

In synchronizing multiple modules using an external clock, one unit is designated as the Master and the other units are designated as Slave units. The external clock is split with low skew and distributed to all units. The Master unit sources the following signals: SYNC clock, and the Sync Marker. These signals are all split and fed to each of the synchronized modules (the Master as well as the Slaves). The

external Sample clock can be in the range of 625 MHz to 1.25 GHz. The Sample clock provides the final retiming of the analog output from each AWG. Any skew in the Sample clock cable delays between the multiple modules will result in the same skew in the analog outputs. Typically, the sample clock signal is split with a matched passive splitter and the cable lengths are matched to better than 5 mm. The resulting skew is small and repeatable. The skew can be measured and calibrated, along with any phase shifts in cables on the ARB outputs, by adding fixed delay offsets to the AWG waveforms. The SYNC clock is used internal to the AWG to clock the internal data generator and to clock in the synchronous triggers. When using the internal clock, the SYNC clock has a frequency of 1/8 of the sample clock rate (156.25 MHz). When synchronizing multiple units, the SYNC clock output must be enabled in software (in the Master) and the external SYNC clock input selected in all the modules. The SYNC clock signal is split passively and distributed with low skew. The SYNC clock output level and the input sensitivity support up to a 1 to 8 split (fan-out) using matched 50 Ohm splitters (6 dB loss per 1 to 2 splitter). There is a specific SYNC cable length that is required as a function of the Sample clock frequency. Several different lengths can be used, provided they are integer multiples of one half of a SYNC clock period.

**Figure 3-9** Cabling Using and External Clock



## Multiple Module Synchronous Trigger Timing

Triggers are registered into the AWG using the SYNC clock. The SYNC clock is nominally at the sample clock frequency divided by 8. However at lower sample rates an internal variable modulus prescaler selects other binary divide ratios: 8, 4, 2, and 1. Multiple AWG synchronization is only supported in the 625 MHz to 1.25 GHz frequency range. The input clock frequency ranges and prescaler divide ratios are as specified in "SYNC Clock Frequency Ranges" on page 91.

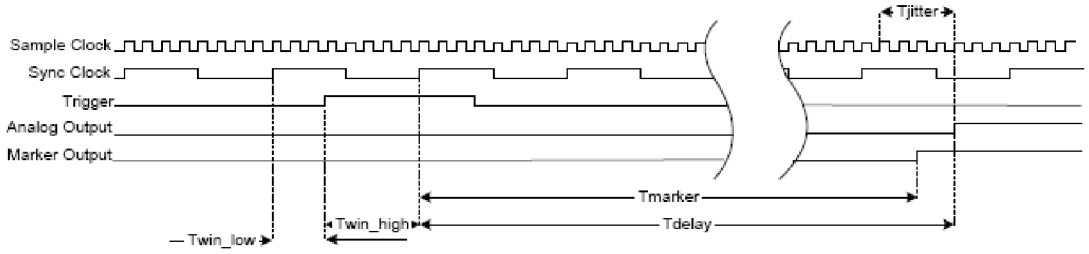
**Table 3-2 SYNC Clock Frequency Ranges**

| Frequency Range | SYNC Clock Prescaler Divide Ratio |
|---|---|
| 625 MHz-1.25 GHz | 8 |
| 312.5 MHz-625 MHz | Multi-Module Synchronization Not Supported |
| 156.25 MHz-312.5 MHz | |
| 100 MHz-156.25 MHz | |

It is necessary to insure that the correct timing relationships are achieved to guarantee consistent synchronous trigger operation. The trigger input must occur within a valid window with respect to the SYNC clock. The window is specified by two times: Twin_low -- the minimum trigger delay after the prior SYNC clock edge; and Twin_high -- the minimum trigger setup before the next SYNC clock edge. These are specified for the trigger Input relative to the SYNC clock Output. The trigger must be a minimum of two SYNC clock cycles long. The trigger timing is specified relative to the rising edge of the SYNC clock by default, as shown in Figure 3-10. To guarantee proper synchronous trigger operation with arbitrary length cables, it is possible to configure the trigger inputs to register the trigger event with respect to the falling edge of the SYNC clock, under software control. In this way there is always a setting for the trigger input timing which will operate reliably for any chosen cable. The typical specifications for the trigger window using the internal clock at 1.25 GS/s is (these values will vary at other clock frequencies):
Twin_high > 3.4 ns

Twin_low > -2.8 ns (the trigger can occur slightly before the prior SYNC clock edge)

**Figure 3-10 Multiple Module Synchronous Trigger Timing Diagram**




## Cable Length and Skew

The cabling requirements are as follows:

**Sample Clock**

Skew less than 10 mm between modules. The absolute SYNC cable length is given by the Equation as a function of the Sample clock frequency:

**Sample Clock Skew Formula**

$$Length = [(n \times 686 \times (1250MHz)/f) - 394]$$

Expressed in mm, where n is an arbitrary integer and f is the sample clock frequency in MHz.

It should be noted that n is the number of 1/2 SYNC clock cycles of total delay between the modules.

This can also be expressed in terms of delay:

$$Cabledelay = \lceil (n \times 3.29 \times (1250MHz)/f) - 1.89 \rceil$$

Expressed in nanoseconds, where n is an arbitrary integer and f is the sample clock frequency in MHz.

For the external Sample clock the formulas apply over the frequency range of 625 MHz to 1.25 GHz

**Marker and Trigger Cables**

The Marker Out to Trigger In cable should be less than 305 mm (12 in). With the 1.25 GHz internal clock, the trigger is falling edge triggered.

# 4 Dynamic Sequencing Option 300

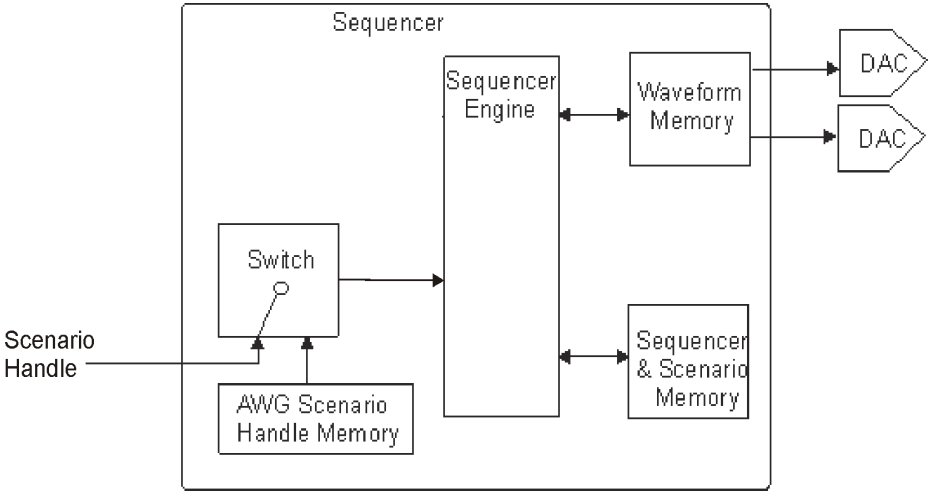
The dynamic sequencing option enables you to access up to eight thousand previously stored scenarios through a 16-bit interface. This functionality gives you the ability to build custom signal scenarios to simulate dynamically changing environments.

# Dynamic Sequencing

Dynamic sequencing is a mode where the AWG scenario handle memory is bypassed and scenarios are selectedfrom an external source. You must first load the data into the N8241A LXI-AWG memory, then, in real-time, provide the scenario handles through the AUX PORT input connector.

**NOTE** The dynamic sequencing option is only available through the programmatic interfaces since it operates in the advanced sequencing mode that is not available through the Control Utility. Refer to "Advanced Sequencing" on page 72.

**Figure 4-1 Dynamic Sequencing Block Diagram**




## AUX PORT Connector

Description: Receptacle, Mini D
Number of Contacts: 20
Manufacturer: 3M
Part Number: 10220-0210EC

**Figure 4-2 AUX PORT Pin Outs**

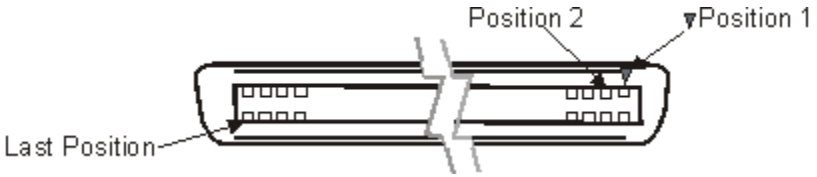



**Table 4-1 Pin Assignment**

| Pin No. | Signal Assignment |
|---|---|
| 1 | Trigger |
| 2 | Ground |
| 3 | Data Valid |
| 4 | CH 1/CH 2 (Reserved, set low) |
| 5 | D0 |
| 6 | D1 |
| 7 | Ground |
| 8 | D2 |
| 9 | D3 |
| 10 | D4 |
| 11 | D5 |
| 12 | D6 |
| 13 | D7 |
| 14 | Ground |
| 15 | D8 |
| 16 | D9 |
| 17 | D10 |
| 18 | D11 |
| 19 | Ground |
| 20 | D12 |

# Signal Levels

All pins are configured as 2.5 V, LVCMOS inputs. The logic levels must be within the following ranges:

| | |
|---|---|
| Low | –0.2 to +0.5 V |
| High | +2.0 to +2.8 V |

# Signal Descriptions

## Data Input

The input data represents a handle to the next scenario to be played by the AWG module. Only the first 8,192 scenarios are available. The scenario handle must be divided by 2 before being written to the AUX port. For example, to play the scenario with a handle of 72, write the value 36 to the AUX port. All scenario handles are even numbers.

## Data Valid

When Data Valid is asserted high, it indicates that the data present on the Data pins is valid and can be latched into the channel 1 and channel 2 next sequence register.

## Trigger

Trigger input can be configured to be either rising-or falling-edge, with a programmable delay. Refer to "Triggers" on page 80.

**NOTE** The latency between trigger assertion and sequence playback is the same as that for the front panel trigger inputs, a resolution of one SYNC clock.

# 5 Direct Digital Synthesis Option 330

The direct digital synthesis (DDS) architecture in the N8241A Series AWGs enables you to create basic waveforms in the AWG memory and then modify the behavior of the waveforms with profiles for amplitude, phase and frequency modulations.

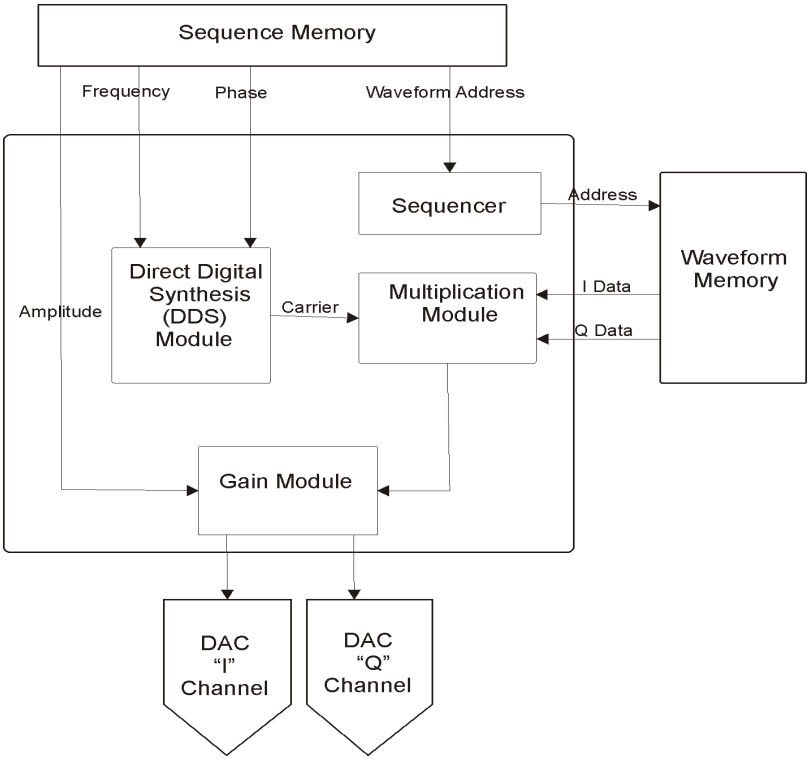
# Direct Digital Synthesis



The N8241A direct digital synthesis application can be managed through the Control Utility graphical user interface (GUI) or one of the supported programmatic interfaces. Accessing DDS through the GUI is the easiest way to view the functionality as many details are handled by the software in the background.

As an introduction, we will step through using DDS with the Control Utility.
Figure 5-1 displays a high level DDS block diagram.

**Figure 5-1 DDS Block Diagram**



# Direct Digital Synthesis Using the Control Utility

**NOTE** A spectrum analyzer is required to display the waveform.

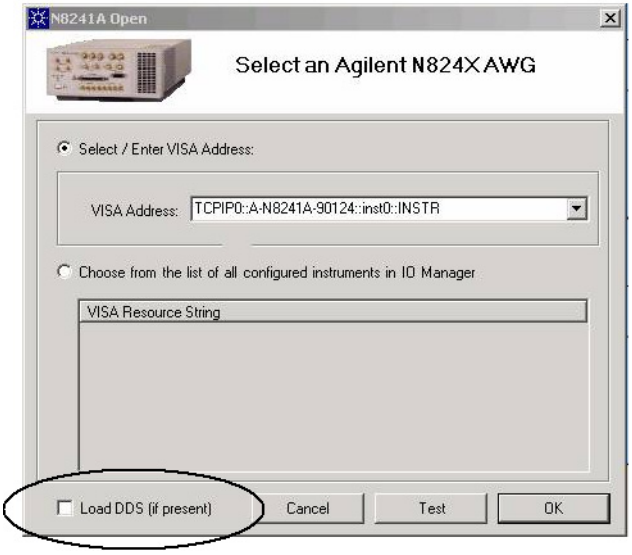


### Configuring the Equipment

1. Connect a 10 MHz reference from the spectrum analyzer to the AWG front panel connector. If you are using a PXI chassis, use the backplane 10MHz reference.
2. Connect the channel 1 positive (+) output to the spectrum analyzer RF input connector.

### Selecting the DDS Option

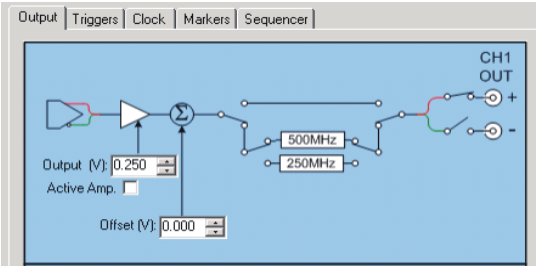
1. Open the **Control Utility** by double-clicking the icon on the desktop.
2. In the **Open Dialog** box, check **Load DDS (if present)**.




### Configuring the Signal Conditioning Path

1. Select the **Output** tab and connect a single-ended signal conditioning path to CH1 OUT (+) (click on the node that you

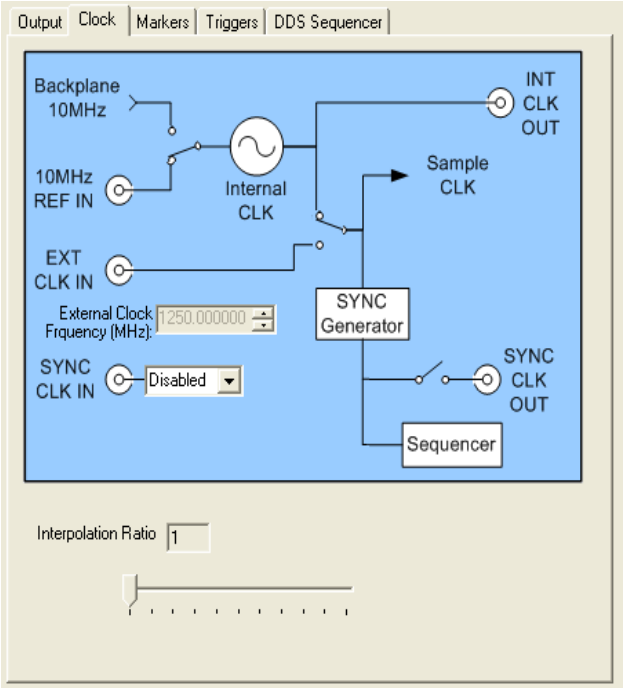
want to connect).




The connection will automatically enable differential mode. Click on the negative (-) node to open this path and enable single-ended mode.

### Configuring the Clock

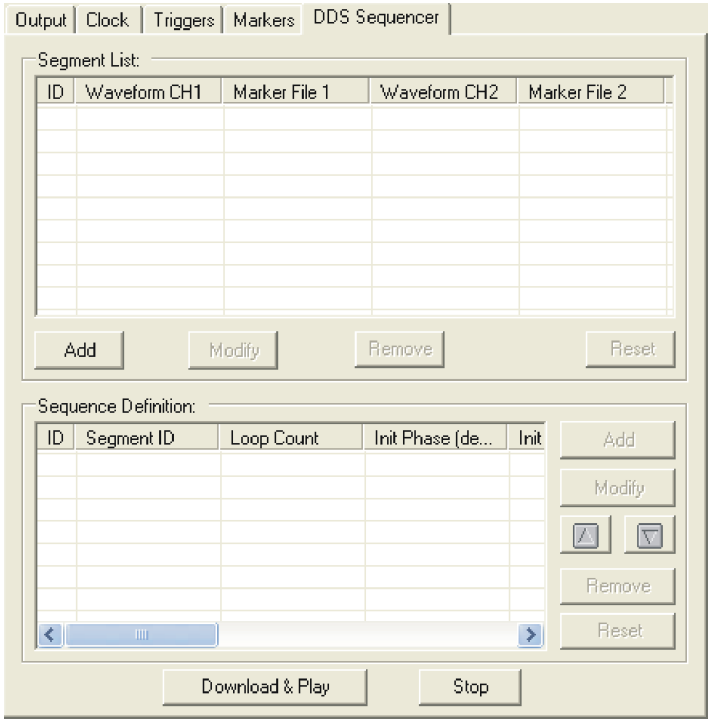
1. Select the **Clock** tab and configure the 10MHz REF IN. For this example, we utilized the 10 MHz reference from the E4440 Spectrum Analyzer in step 1. If you are using a PXI chassis, leave the clock set to the default Backplane 10MHz.



2. Use the default setting for the **Interpolation Ratio**.

### Configuring the Sequencer

1. Select the **DDS Sequencer** tab.

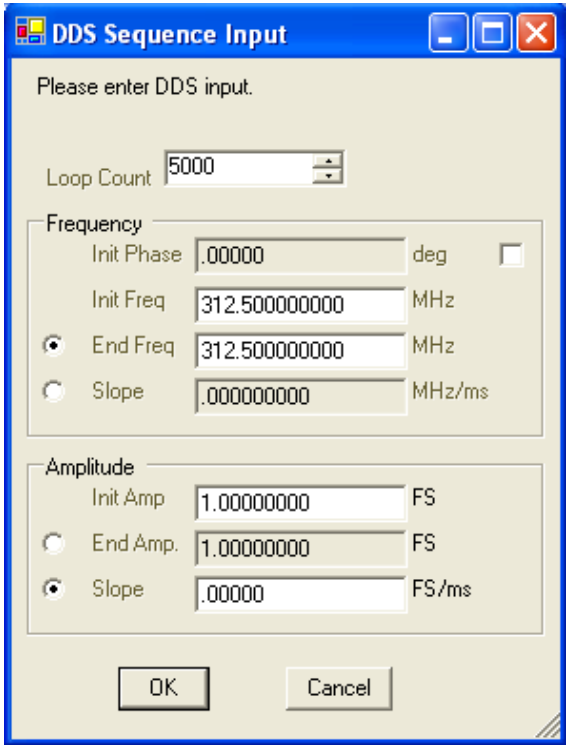



2. From the **Segment List** select **Add**. This brings up a **Segment Information** window.
3. Browse and select the **DDS_All_Ones** waveform from the **Demo Waveform DDS** folder included on the N8241A Series CD or the memory stick, then click **OK**.

**NOTE** For dual channel sequencing, add waveforms of the same length to both channel 1 and channel 2. Currently, the software does not support independent channel sequencing.

4. In the **Segment List**, select the **DDS_All_Ones** waveform.

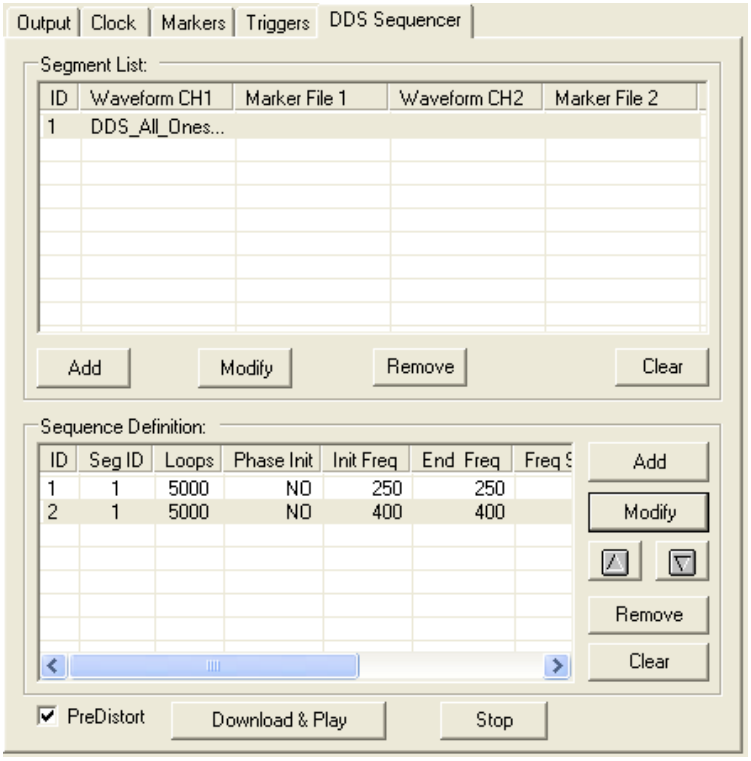
5. In the **Sequence Definition** area, select **Add**. This brings up the
**DDS Sequence Input** window.
6. Enter **5000** repetitions and accept all default settings. Click **OK**.




**NOTE** The values entered in the DDS Sequence Input window are recorded in the sequence definition area of the Sequencer tab. This enables you to review the values after the DDS Sequence Input window is closed.

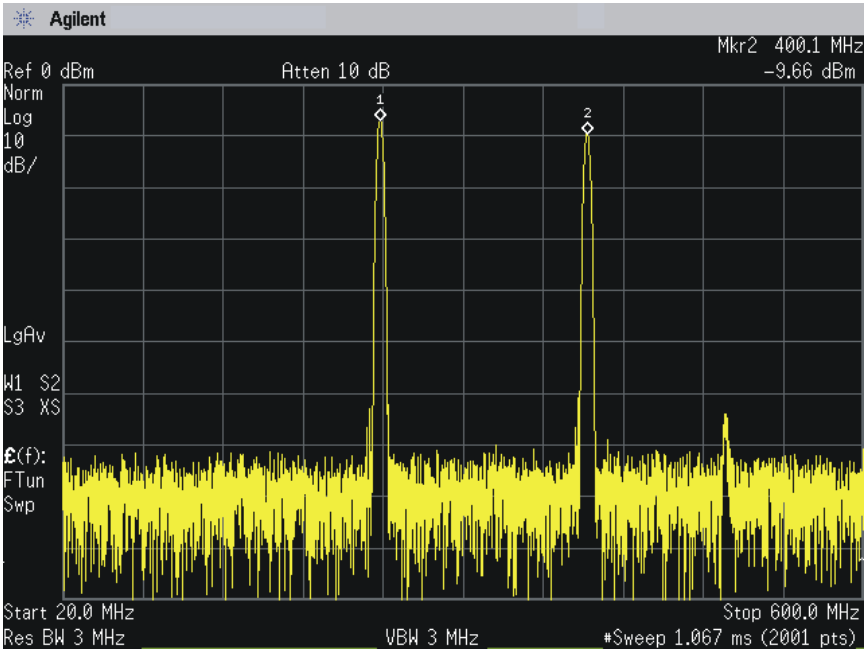
7. Repeat steps **4**, **5**, and **6** using a 400 MHz Init Freq Value.
8. The sequencer tab should look like Figure 5-2.

**Figure 5-2 Sequencer Tab**




9. Click **Download & Play**. The spectrum of the sequence should be similar to the one shown in Figure 5-3.

**Figure 5-3 Playback of a Sequence**

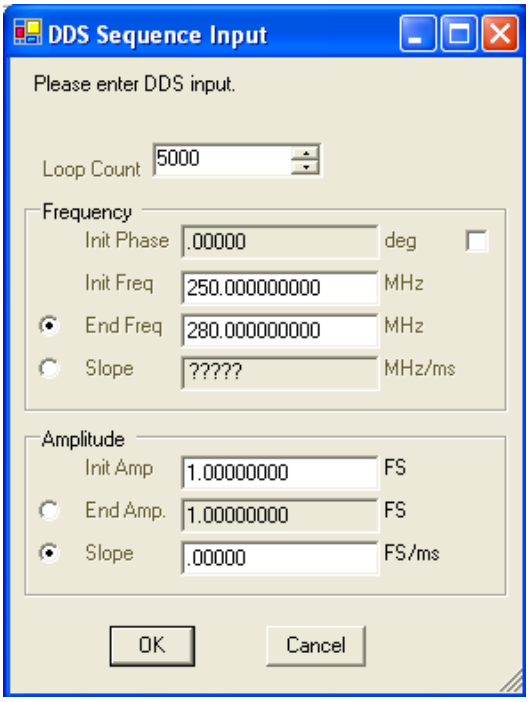



The 250 MHz carrier (marker 1) and the 400 MHz carrier (marker 2) are combined with a waveform composed of all ones.This illustrates how the DDS engine produces sine waves when a constant frequency is specified.

### Out of Range Input Values

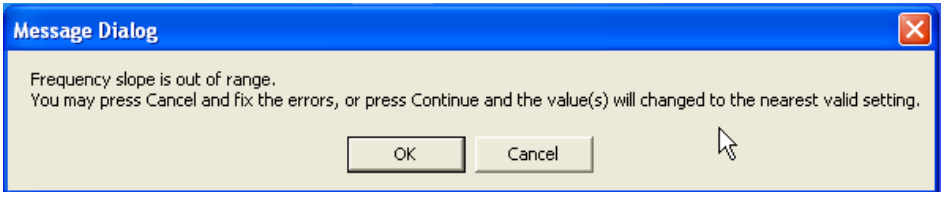
Some values may cause an 'out of range' condition. Refer to Figure 5-4.

**Figure 5-4 DDS Sequence Input Window**



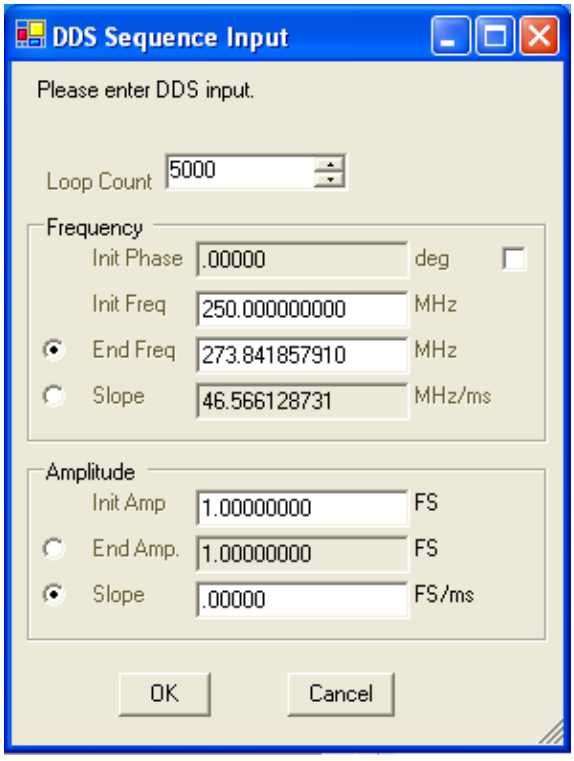

Notice the question marks in the **Frequency Slope** box. This is occurs when the combination of the loop count, the initial frequency, and the end frequency cannot be calculated correctly. If you select **OK**, a message window comes up.

**Figure 5-5 Message Dialog**




For this example, selecting **OK** resulted in values shown in Figure 5-6.

**Figure 5-6 Calculated Valid Settings**




The end frequency value was adjusted to enable the slope count.

**NOTE** This type of 'out of range' condition may also occur with amplitude settings.

# Theory of Operation

The Direct Digital Synthesis, Option 330, is a powerful tool for those customers who are using the N8241A Arbitrary Waveform Generator (AWG) to synthesize waveforms best expressed in the frequency domain. Traditionally, waveforms are expressed in the time domain, sampled, and then stored in waveform memory for eventual playback. This approach is completely generic and applicable to any describable waveform. However, many waveforms can be described as a combination of information content and simple sinusoids. For these waveforms, most of the available waveform memory gets used up storing the sinusoids, leaving little space for the information content.This is an inefficient utilization of waveform memory.

For example, in communications, the waveform can be described as a carrier (sinusoid) modulated with data (information content). Because the AWG has such high dynamic range, the modulated carrier can be generated with very good equivalent error vector magnitude (EVM) performance. But, because the carrier has to be stored in waveform memory along with the modulation, limited playback time can be achieved. Another important example of a frequency domain waveform is wideband radar chirps. Again, the waveform consists of a combination of a sinusoid and a frequency chirp profile, both of which must be traditionally stored in waveform memory, resulting in limited playback time.

To address this issue, Option 330 allows the AWG to generate the sinusoidal portion of the waveform real time, and then modulate the sinusoid with the information content stored in waveform memory (see Figure 5-7). This is done by adding a direct digital synthesizer (DDS) to the main FPGA in the AWG. The DDS implemented has a frequency resolution of 1.1369 mHz, and can synthesize sinusoids from DC to 400 MHz (using the 1.25 GHz internal clock). The DDS can be linearly ramped in frequency, with a frequency ramp rate resolution of 1.3552 Hz/s, and a maximum frequency ramp rate of 46.566 GHz/s. The frequency ramp rate can be positive or negative.

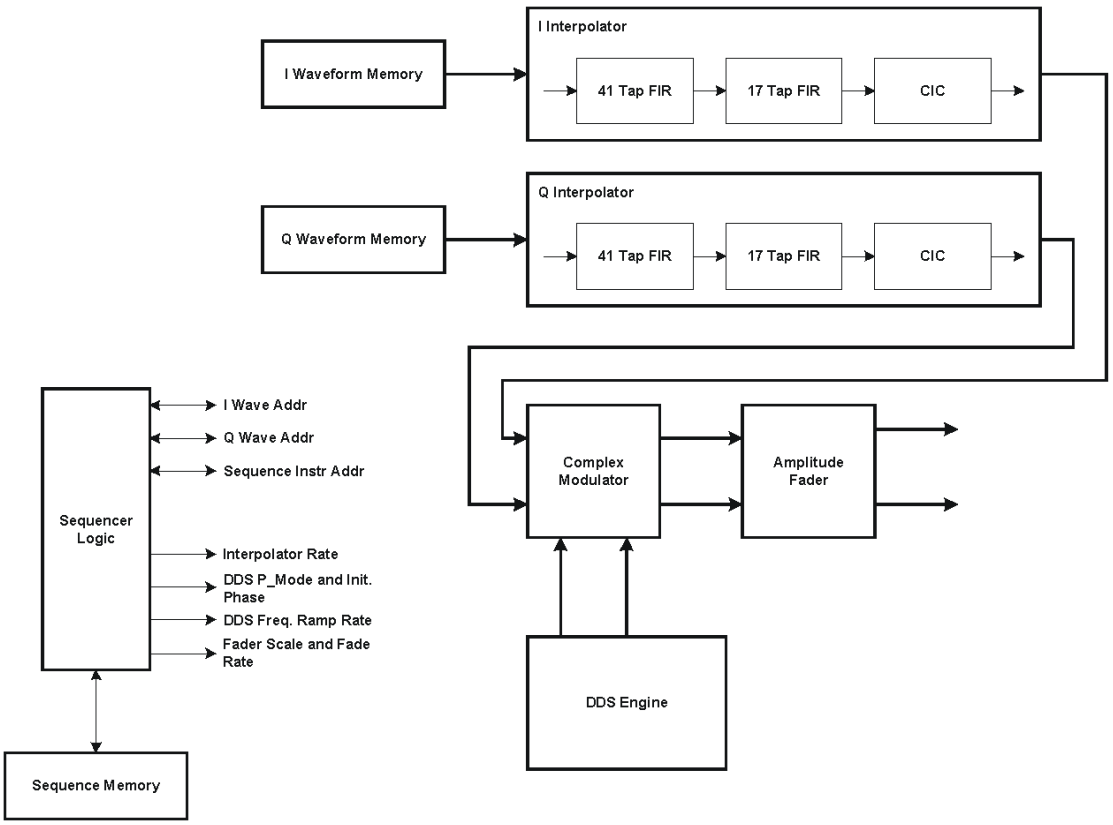
The initial phase of the DDS can be set to a known value, with a phase resolution of 21.458 µdegrees. Alternatively, through the use of the initial phase control field, the DDS can be operated in phase continuous mode; for example, the initial phase not initialized. This is useful for applications requiring phase continuous frequency hopping. The DDS generates both sine and cosine outputs for use in the complex modulator. Refer to Figure 5-7.

To allow waveform memory to be played back at a rate slower than the AWG sample rate, interpolation filters have been added to the main FPGA, for both channels. The interpolation filters can be configured to interpolate by integer powers of two: 2, 4, 8. . ., up to a value of 1024. Image rejection for the filters is better than 65 dBc for all interpolation rates, and flatness is compensated for automatically in software. By setting the interpolation filters to 1024, the waveform memory can be played back at a rate over a thousand times slower than the AWG sample rate. The interpolation filters can also be bypassed.

The sine and cosine outputs of the DDS, and the interpolated outputs of waveform memory are sent to a complex (or I/Q) modulator for upconversion. If the channel 1 interpolated memory is represented symbolically by “I”, and the channel 2 interpolated memory by “Q”, then the channel 1 analog output can be expressed as I*cos(wt) – Q*sin(wt).
Channel 2 can be expressed as I*sin(wt) + Q*cos(wt). Each analog output represents a carrier (DDS output) I/Q modulated by data (channel 1 and 2 interpolated waveform memory). Alternatively, if both analog channels are subsequently used to drive an external I/Q modulator, they are configured to provide for upper sideband SSB conversion at the output of the external modulator.

Both internally modulated outputs can be linearly faded in amplitude within the AWG. The linear fade function occurs after the complex modulator. Amplitude fade rate resolution is set to 1.819% full scale per second, with a maximum fade rate of 62.5% full scale per nanosecond. Fade rates can be positive or negative.

**Figure 5-7 DDS**



# 6 Troubleshooting

The following topics are included in this chapter.

# Software

## Removing the Software

If it is necessary to remove the N8241A software, go to:

**Start > Settings > Control Panel > Add/Remove Programs**

1. Select **Agilent N8241A AWG (Version)**, then select **Remove.**
2. You may need to restart the PC, but this will completely remove all of the files.

## Moving the Software

If it becomes necessary to move the N8241A software, complete the instructions documented in Removing the Software. Then, using the N8241A CD, reinstall the software where it is needed.

## Updating the Software

To resolve an error message you get while attempting to upgrade the N8241A software, take the following steps in the listed order:

1. Go to: **Start > Settings > Control Panel > Add/Remove Programs**
2. Select **Agilent N8241A AWG (Version)**, then select **Remove.**
3. You may need to restart the PC, but this will completely remove all of the files.
4. Reinstall the N8241A software.

# Initializing the LAN Configuration

On the front of the instrument, near the power switch, is a recessed button labeled “RST”. This button enables you to put the LAN configuration of the instrument into a known state. This is useful if the LAN address gets set to an unknown value.

When you press this button (a straightened paper clip will do the job) the following settings are made and the system reboots:

- IP Address is set to 192.168.EE.FF, where EE and FF are the last two parts of the MAC address (AA.BB.CC.DD.EE.FF). This is designed to prevent multiple instruments from using the same default IP address.
- Subnet Mask is set to 255.255.0.0
- DHCP is set to ON
- Auto IP i set to ON
- The instrument hostname is set to A-N82XXA-NNNNN, where N82XXA is the instrument model number (such as N8241A) and NNNNN represents the last five digits of the instrument serial number.

If the instrument is in an environment with a DHCP server, it is assigned an IP address through DHCP. The IP address can be found by using the instrument name as the URL. Generally, a web browser will find the instrument.

Without the DHCP, the instrument will use Auto IP and acquire a 169.254.*.* address. If no DHCP is present, but the instrument is set to use DHCP (the default), the instrument will wait two minutes for its DHCP to time out. In this case, there is a time delay of approximately three minutes between when the instrument is powered on and when it is usable.

# Contacting Agilent

By internet, phone, or fax, get assistance with all your test and measurement needs.

**Table 6-1 Contacting Agilent**

**Online assistance:** http://www.agilent.com/find/assist

| **United States** | **Latin America** | **Canada** | **Europe** |
|---|---|---|---|
| (tel) 1 800 452 4844 | (tel) (305) 269 7500<br>(fax) (305) 269 7599 | (tel) 1 877 894 4414<br>(fax) (905) 282-6495 | (tel) (+31) 20 547 2323<br>(fax) (+31) 20 547 2390 |
| **New Zealand** | **Japan** | **Australia** | |
| (tel) 0 800 738 378<br>(fax) (+64) 4 495 8950 | (tel) (+81) 426 56 7832<br>(fax) (+81) 426 56 7840 | (tel) 1 800 629 485<br>(fax) (+61) 3 9210 5947 | |

**Asia Call Center Numbers**

| Country | Phone Number | Fax Number |
|---|---|---|
| **Singapore** | 1-800-375-8100 | (65) 836-0252 |
| **Malaysia** | 1-800-828-848 | 1-800-801664 |
| **Philippines** | (632) 8426802<br>1-800-16510170 (PLDT Subscriber Only) | (632) 8426809<br>1-800-16510288 (PLDT Subscriber Only) |
| **Thailand** | (088) 226-008 (outside Bangkok)<br>(662) 661-3999 (within Bangkok) | (66) 1-661-3714 |
| **Hong Kong** | 800-930-871 | (852) 2506 9233 |
| **Taiwan** | 0800-047-866 | (886) 2 25456723 |
| **People's Republic of China** | 800-810-0189 (preferred)<br>10800-650-0021 | 10800-650-0121 |
| **India** | 1-600-11-2929 | 000-800-650-1101 |

## Returning the Instrument to Agilent

If it becomes necessary to return the N8241/2A AWG to the factory, use the original or comparable packaging.

# 7 Technical Characteristics

The following topics are included in this chapter.

# Technical Characteristics

## Channels

Two independent channels available as baseband or IF outputs

CH1: Single-ended and differential

CH2: Single-ended and differential

## Modulation bandwidth

500 MHz per channel (1 GHz IQ bandwidth)

## Resolution

N8241A: 15 bits

N8242A: 10 bits

## Output spectral purity (CH1 and CH2)

### Harmonic Distortion: 1 kHz to 500 MHz

- N8241A < -65 dBc for each channel
- N8242A < -50 dBc for each channel

### Non-Harmonic Distortion: 1 kHz to 500 MHz

- N8241A < -65 dBc for each channel
- N8242A < -65 dBc for each channel

### Noise floor

- N8241A < -150 dBc/Hz across the channel bandwidth
- N8242A < -150 dBc/Hz across the channel bandwidth

### Sample clock

- Internal: Fixed 1.25 GS/s
- Internal clock output: +3 dBm nominal into 50 ohm load
- External clock input: Tuneable 100 MS/s to 1.25 GS/s
- External clock input (power): -15 to +5 dBm, 0 dBm nominal

### Phase Noise Characteristics

- 1 kHz -95 dBc/Hz
- 10 kHz-115 dBc/Hz
- 100 kHz-138 dBc/Hz
- 1 MHz-150 dBc/Hz
- Noise Floor-150 dBc/Hz

### Accuracy: Same as 10 MHz timebase input

## 10 MHz REF IN

- Input drive level: –5 to +10 dBm into 50 ohms (nominal)

## 10 MHz REF OUT

- Output drive AC-coupled: 50 ohms (+5 dBm nominal)

## AUX 10 MHz Frequency reference in

- Input drive level: +2 to +12 dBm into 50 ohms (+2 dBm nominal)

## Waveform length

- 8 MS per channel (16 MS with option 016)
- Minimum waveform length: 128 samples
- Waveform granularity: 8 samples

## Segments

From 1 to 32,768 unique segments can be defined consisting of waveform start and stop address, repetitions and marker enable flags.

## Sequences

Up to 16,384 total unique waveform segments can be combined with separate loop counts to form a sequence.

## External triggers

### Front Panel

- Triggers 1/2/3/4
- Number of inputs: 4 SMB female front-panel connectors
- Trigger polarity: Negative/positive
- Trigger impedance: 2k ohms
- Maximum input level: 4.3V
- Input sensitivity: 250 mV
- Trigger threshold: -4.5 to + 4.5 V
- Trigger timing resolution: Clock/8 (6.4 ns at full rate)
- Trigger uncertainty: < 50 ps
- Minimum trigger width: 12.8 ns at full clock rate
- Trigger delay: resolution of 1 SYNC clock

### Trigger In*

- Trigger impedance: 4k ohms
- Trigger level:LVTTL

*Trigger In has additional latency.

### LXI Trigger Bus

- All physical and electrical characteristics conform to LXI Standard Revision 1.1.

## External markers

Markers can be defined for each waveform segment.

### Front Panel

### Markers 1/2/3/4

- Number of outputs: 4 SMB female front-panel connectors
- Marker polarity: Negative, positive
- Output type: 3.3V CMOS with 30 ohm series termination
- Marker low level: 100 mV nominal (high impedance load)
- Marker high level: 3.2V nominal (high impedance load)
- Marker timing resolution: Clock/8 (6.4 ns at full rate)
- Marker delay: resolution of 1 sample clock
- Marker width: resolution of 1 SYNC clock

### Trigger Out*

- Output type:5V TTL with 50 ohm termination
- Marker low level: 100 mV nominal (high impedance load)
- Marker high level: 4.9V nominal (high impedance load)

- 2.4V nominal when terminated into a 50 ohm load

*Trigger Out has additional latency.

## LXI Trigger Bus

- All physical and electrical characteristics conform to LXI Standard Revision 1.1

## Module synchronization

- Hardware supports synchronization of multiple AWGs with future software enhancements.
- Sync clock output level: 800 mVp-p 50 ohm output impedance, AC coupled
- Sync clock input level: 100 mVp-p into 50 ohms AC coupled

## Analog output

- Output connector: SMA female
- Output impedance: ~50 ohms

## Analog output levels

The following output levels are specified into 50 ohms

- Uncorrected passband flatness: +/- 1 dB DC - 200 MHz;
- Passive Mode Differential: +/- 3.5 dB DC - 500 MHz (with 1.25 GHz clock)

- Uncorrected passband group delay: +/- 500 ps DC - 200 MHz; +/- 1 ns DC - 500 MHz (with 1.25 GHz clock)
- Single-Ended Passive Mode: 0.5Vp-p
- Differential Passive Mode: 1.0Vp-p with ±0.047Vp-p
- Single-Ended Active Mode1.0Vp-p with ±0.2Vp-p
- Differential Active Mode: N/A

## Reconstruction filters

- 500 MHz and 250 MHz realized as 7-pole elliptical filters plus thru-line output

# General Characteristics

## Power

**Line power:**

100/120/220/240 V AC, 50/60 Hz, 100 Watts maximum

## Environmental

Samples of this product have been type tested in accordance with the Agilent Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation, and End-use; those stresses include but are not limited to temperature, humidity, shock vibration, altitude, and power line conditions. Test methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

- Operating temperature: 0 to +50 degrees C (0 to 47 degrees C at 15,000 ft altitude)
- Storage temperature: –40 to +70 degrees C

**Relative Humidity**

- Type tested: 0% to 95% at 40 degrees C (non-condensing)
- Altitude: 0 to 4500m (15,000 ft) above sea level

## Weight

- 5.66 kg (12.5 lb)

## Security

- All user data stored in volatile memory

## Dimensions

- Height: 89 mm (3.5 inch)
- Width: 213 mm (8.375 inch)
- Depth: 422 mm (16.625 inch)

## Recommended calibration cycle

- 12 months

## ISO compliance

This instrument is manufactured in an ISO-9001 registered facility in concurrence with Agilent Technologies, Inc. commitment to quality.

- Electrostatic Discharge Immunity - IEC 61000-4-2: passes criterion C

Testing according to IEC 61000-4-2: showed that the exposure of the data port to electrostatic discharge may interrupt operation of the N8241/2A. Operation can be restored by reloading the desired waveforms and restarting. This required operator intervention results in a criterion C classification.

## Options

- N8241A-016: Waveform memory expansion to 16 MS per channel
- N8241A-300 Dynamic Sequencing
- N8241A-330 Direct Digital Synthesis (DDS)

# Index